FIG. 1

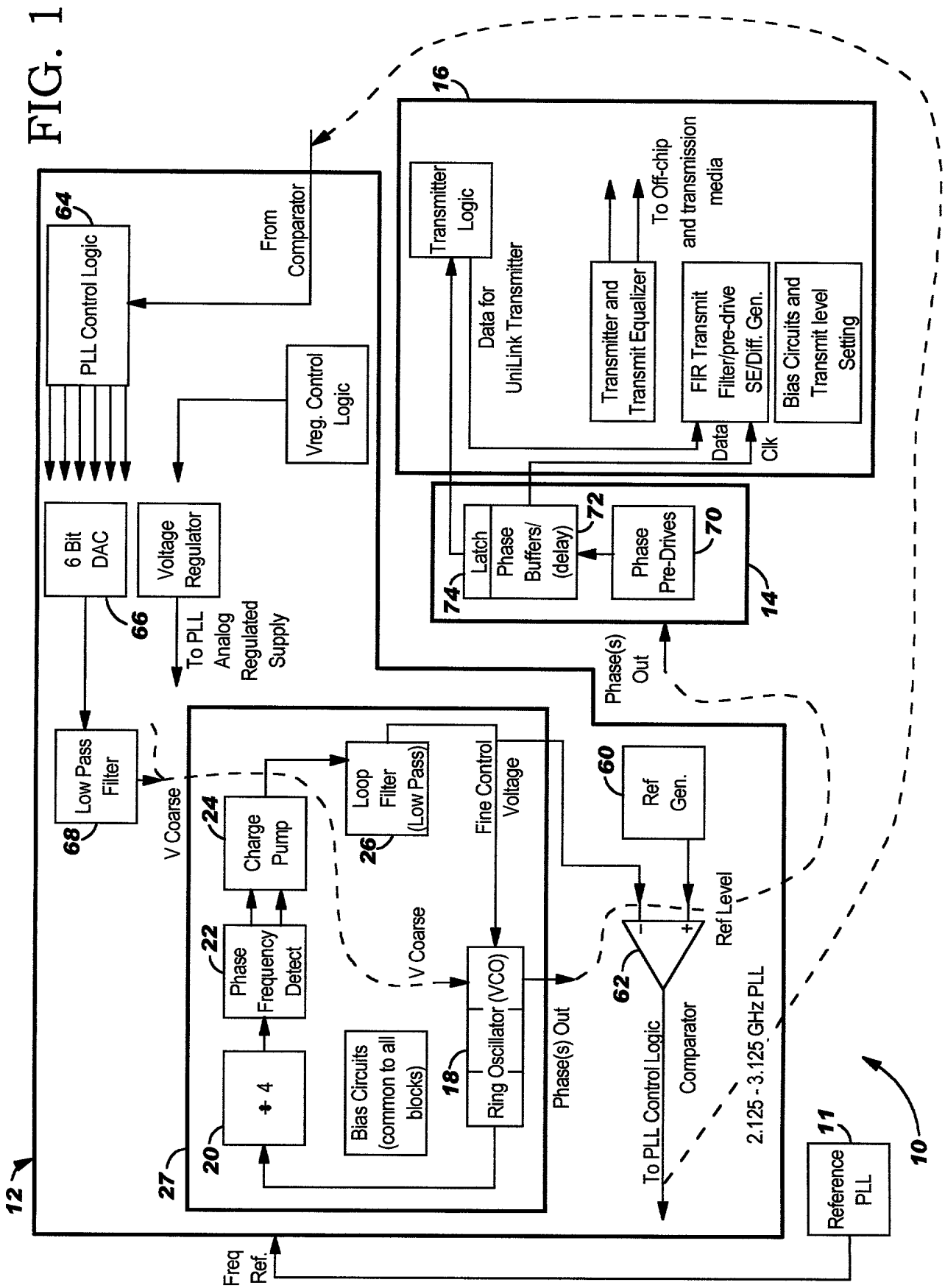
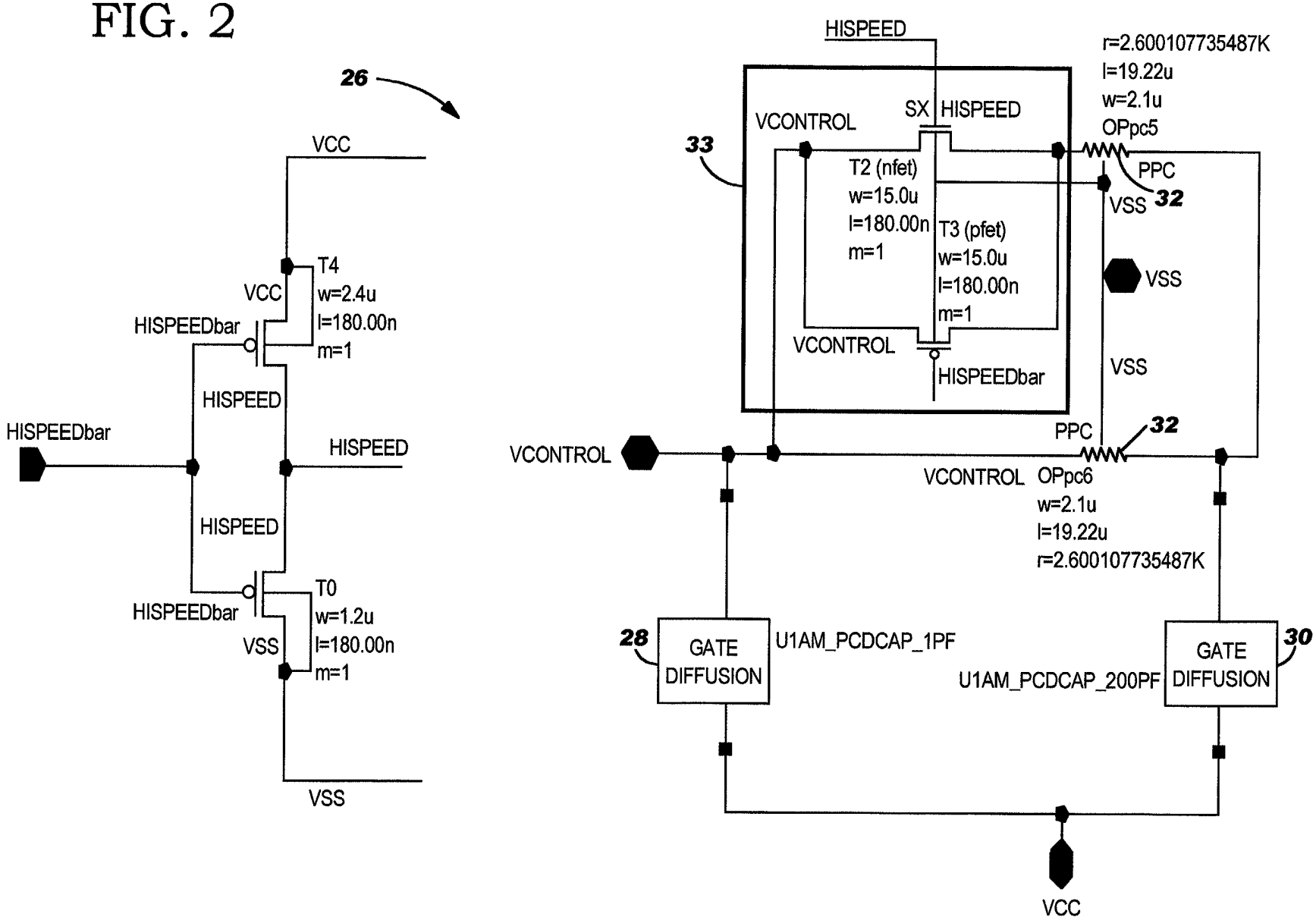

12
16
64
PLL Control Logic
From Comparator
Vreg. Control Logic
Transmitter Logic
Data for UniLink Transmitter
Transmitter and Transmit Equalizer
To Off-chip and transmission media
FIR Transmit Filter/pre-drive SE/Diff. Gen.
Bias Circuits and Transmit level Setting
Data
Clk
6 Bit DAC
66
Voltage Regulator
To PLL Analog Regulated Supply
72
Latch
Phase Buffers/ (delay)
74
Phase Pre-Drives
70
14
Phase(s) Out
Low Pass Filter
68
V Coarse
24
Charge Pump
26
Loop Filter (Low Pass)
Fine Control Voltage
60
Ref Gen.
22
Phase Frequency Detect
V Coarse
Bias Circuits (common to all blocks)
18
Ring Oscillator (VCO)
Phase(s) Out
62
Ref Level
+ 4
20
27
To PLL Control Logic
Comparator
2.125 - 3.125 GHz PLL
11
Reference PLL
10
Freq Ref.

FIG. 2



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FIG. 3

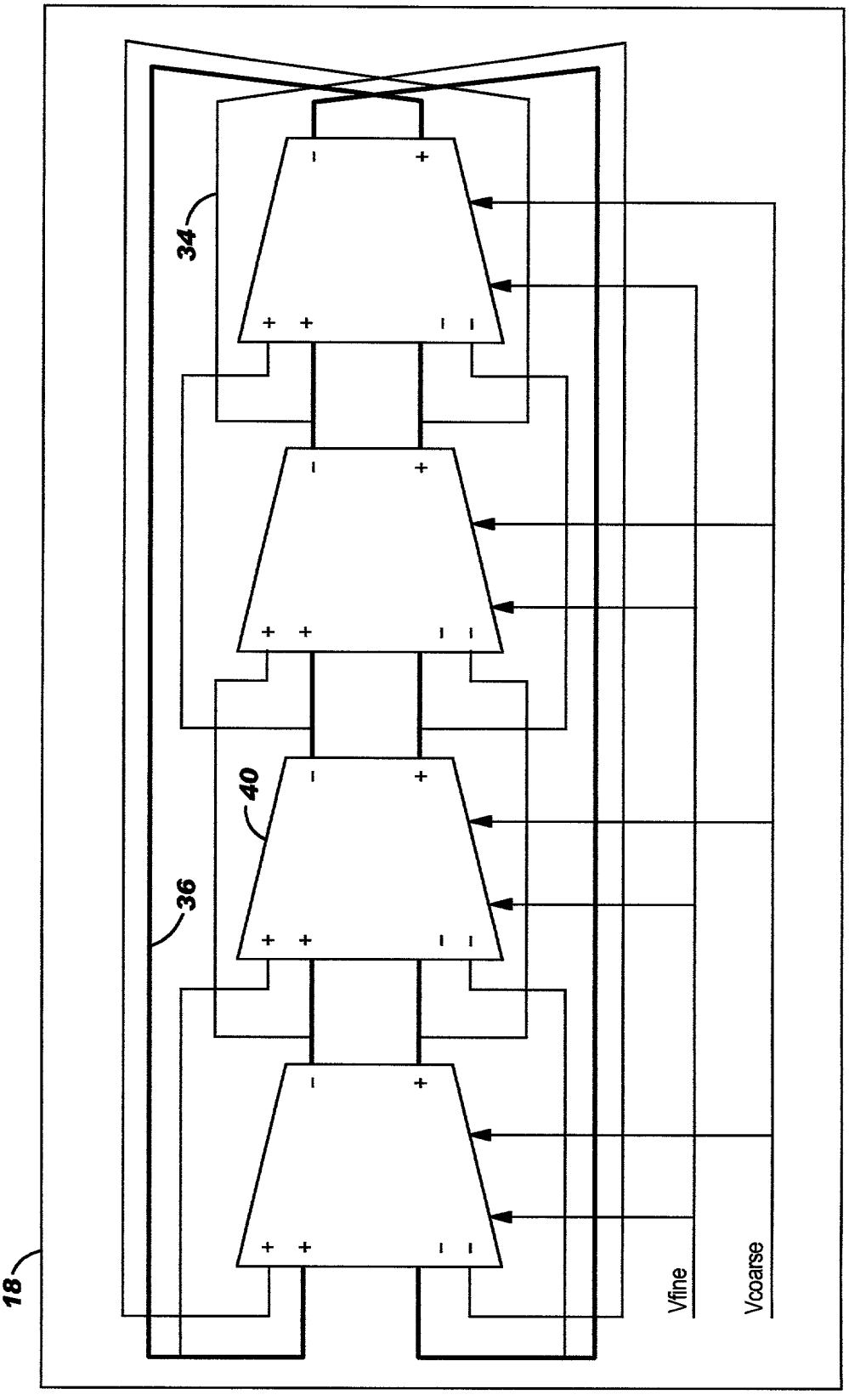
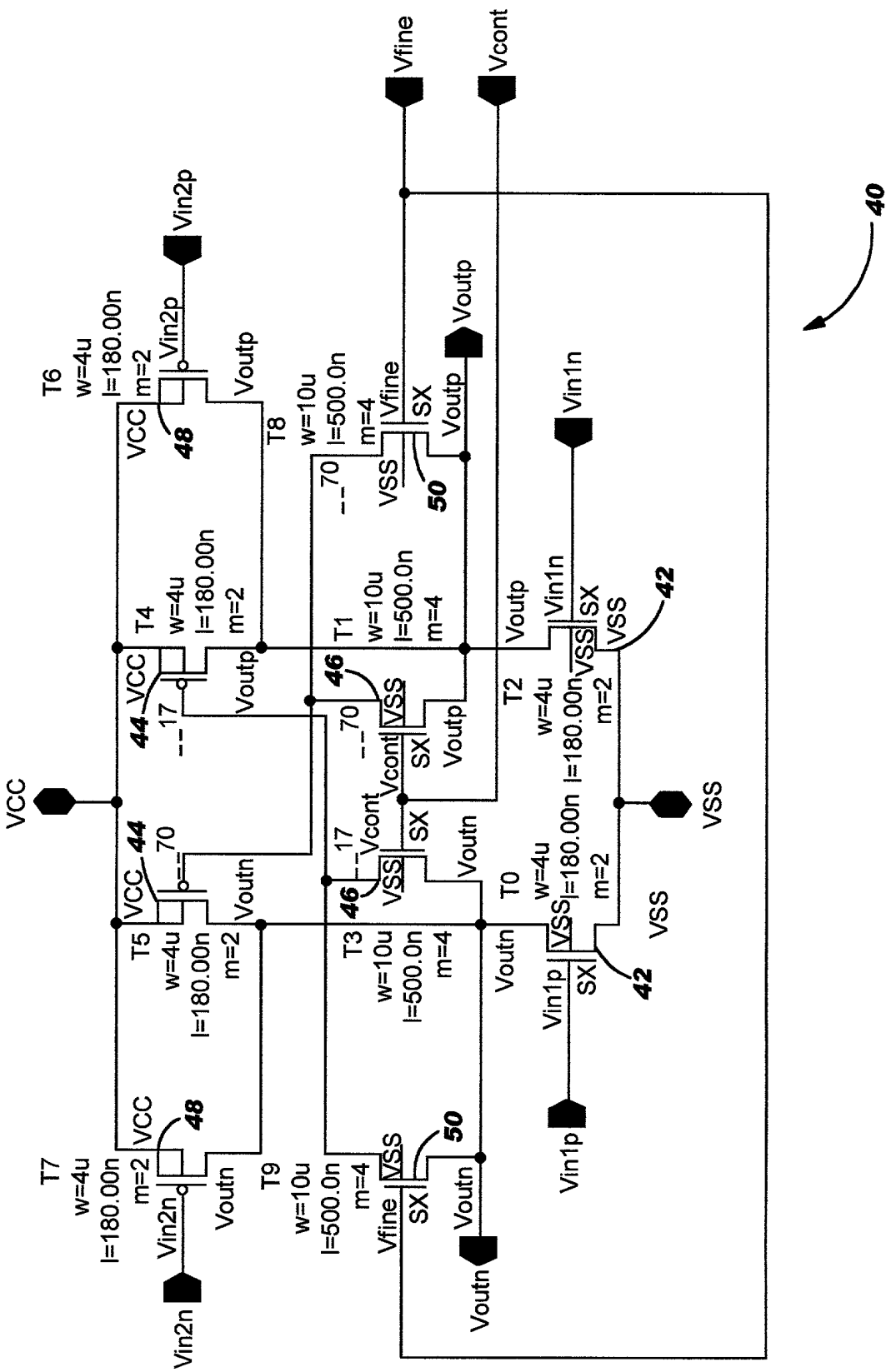


FIG. 4


VCC
Vfine
Vcont
Vin2p
Vin2n
Vin1n
Vin1p
Voutp
Voutn
VSS
40
42
44
46
48
50
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
w=4u
l=180.00n
m=2
w=10u
l=500.0n
m=4
SX

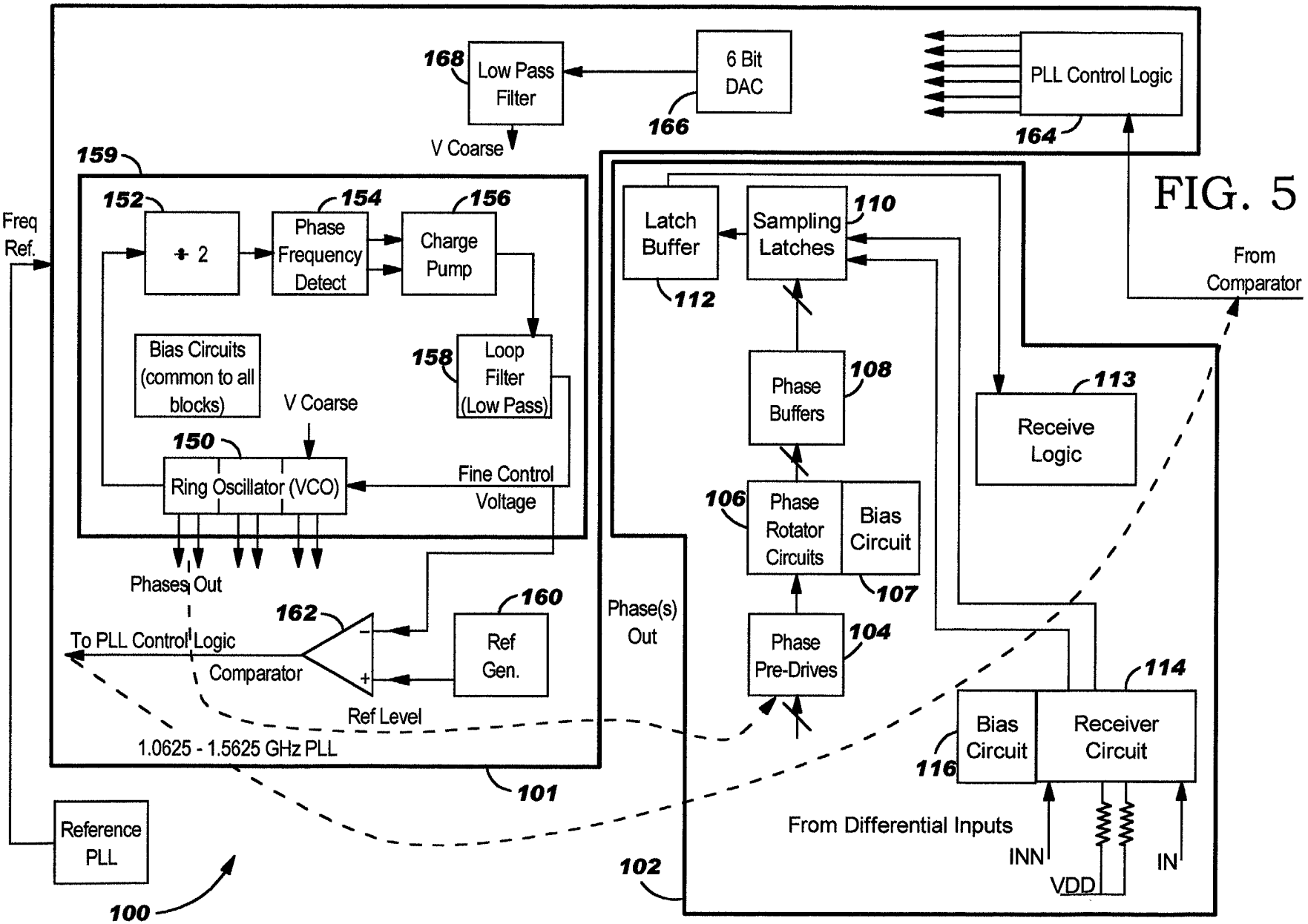


FIG. 5

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FIG. 6

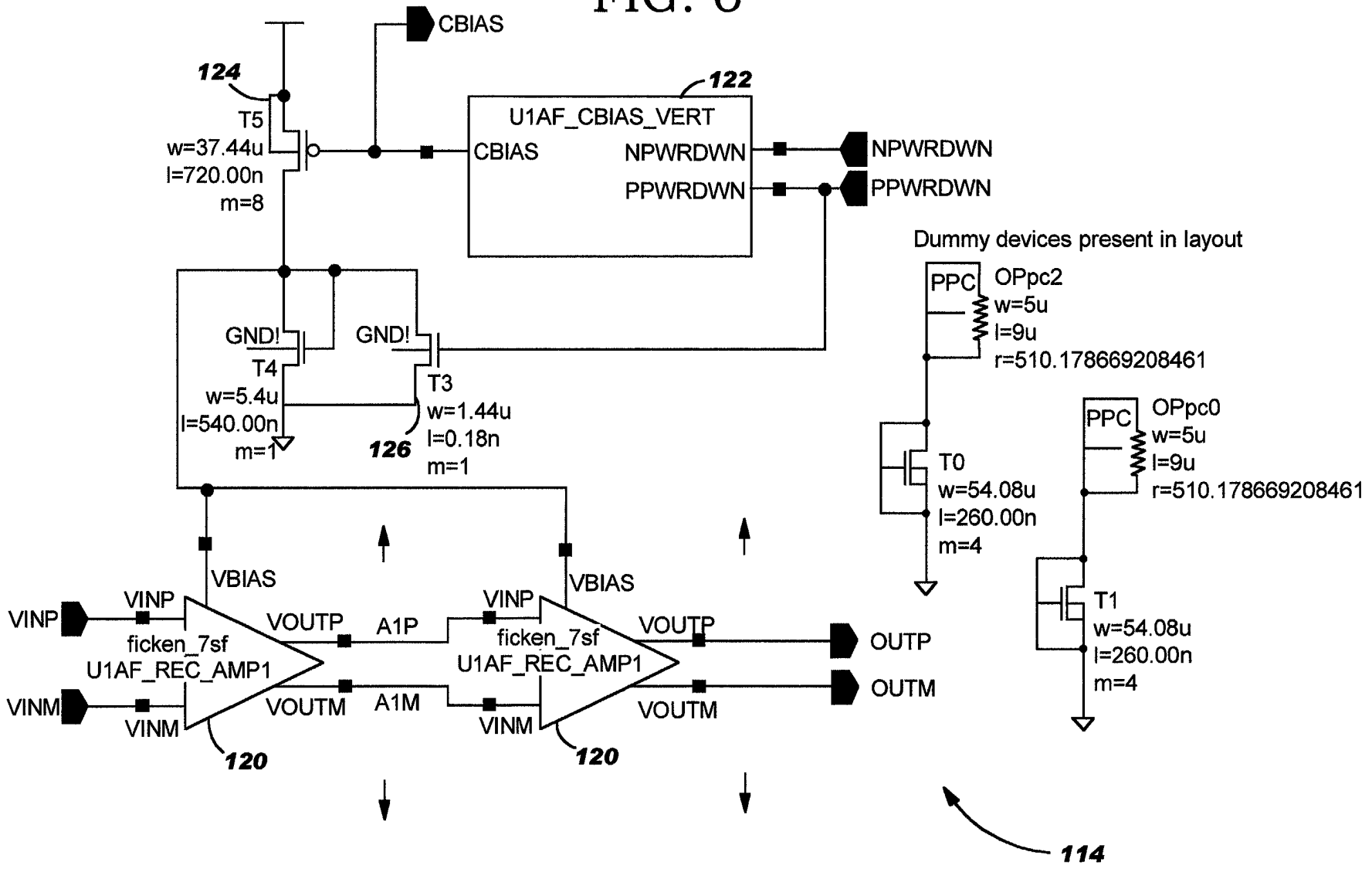

CBIAS
124
122
T5
w=37.44u
l=720.00n
m=8
U1AF_CBIAS_VERT
CBIAS
NPWRDWN
PPWRDWN
NPWRDWN
PPWRDWN
Dummy devices present in layout
PPC
OPpc2
w=5u
l=9u
r=510.178669208461
GND!
GND!
T4
w=5.4u
l=540.00n
m=1
T3
w=1.44u
l=0.18n
m=1
126
T0
w=54.08u
l=260.00n
m=4
PPC
OPpc0
w=5u
l=9u
r=510.178669208461
T1
w=54.08u
l=260.00n
m=4
VBIAS
VBIAS
VINP
VINP
VINP
VOUTP
A1P
ficken_7sf
U1AF_REC_AMP1
ficken_7sf
U1AF_REC_AMP1
VOUTP
OUTP
VINM
VINM
VOUTM
A1M
VINM
VOUTM
OUTM
120
120
114

FIG. 7

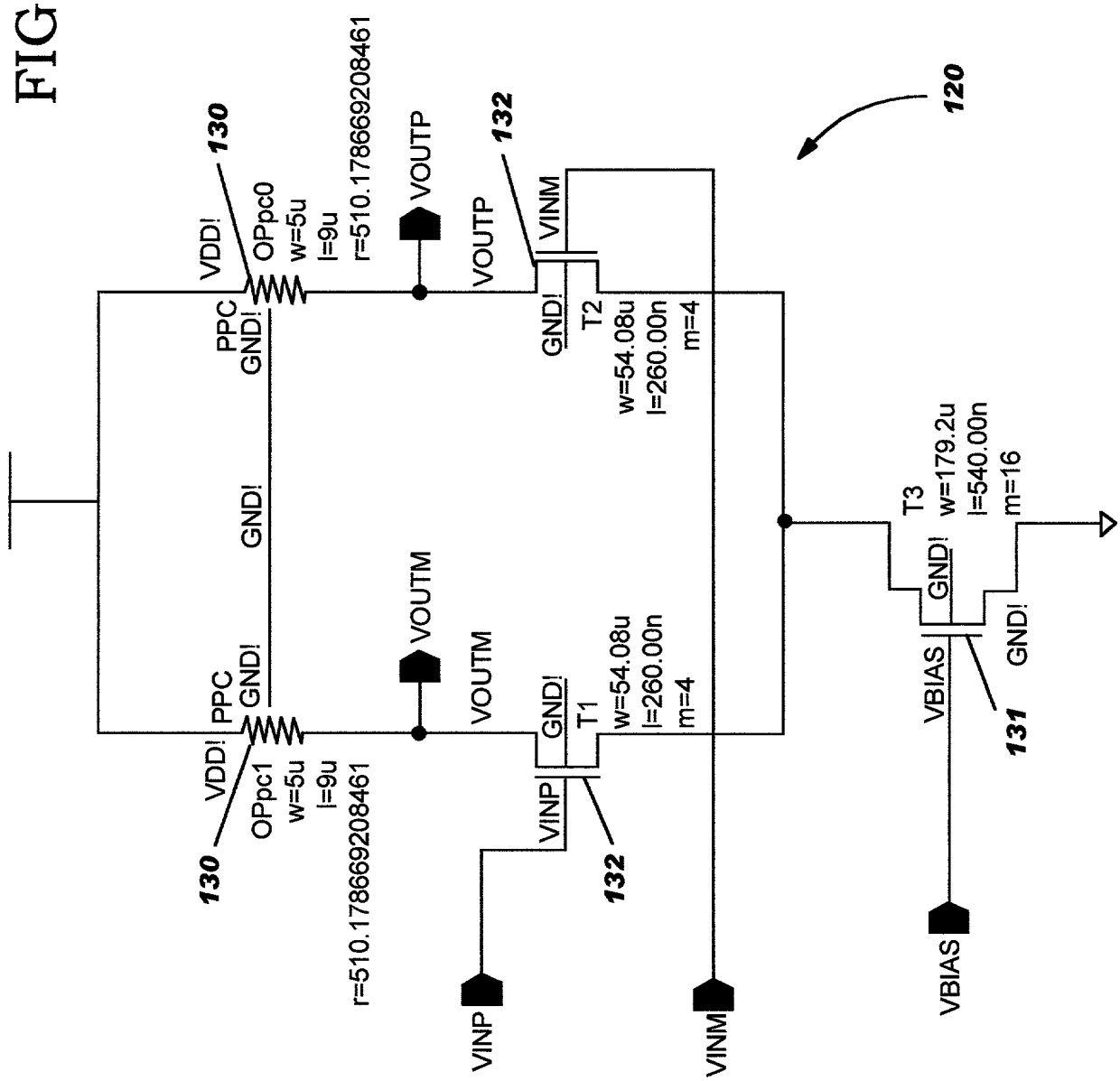
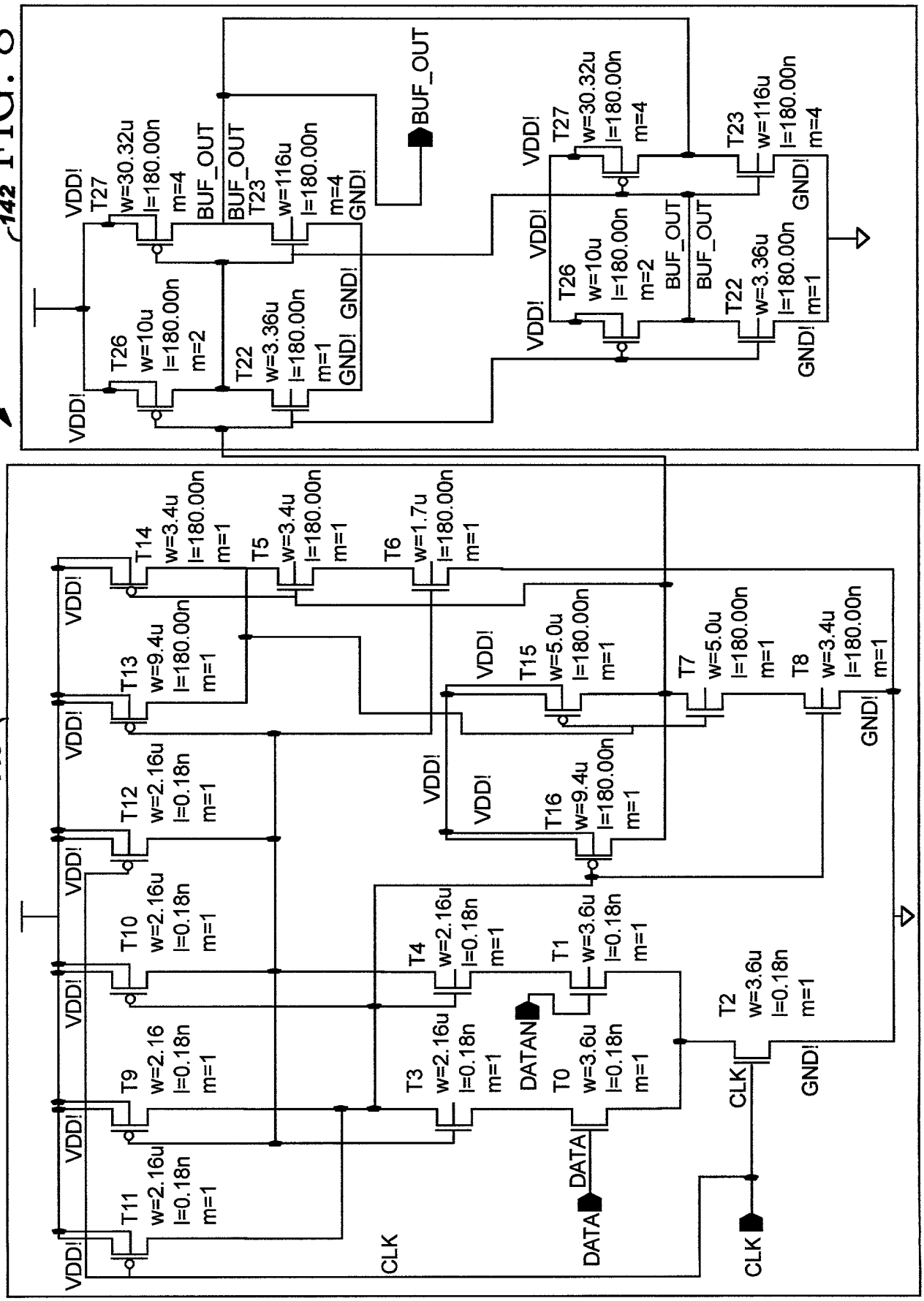

120
130
VDD!
OPpc0
w=5u
l=9u
r=510.178669208461
PPC
GND!
VOUTP
132
VINM
T2
w=54.08u
l=260.00n
m=4
GND!
VOUTM
VINP
T1
w=54.08u
l=260.00n
m=4
T3
w=179.2u
l=540.00n
m=16
VBIAS
131

FIG. 8


110
142
140
VDD!
GND!
BUF_OUT
T27 w=30.32u l=180.00n m=4
T26 w=10u l=180.00n m=2
T23 w=116u l=180.00n m=4
T22 w=3.36u l=180.00n m=1
T14 w=3.4u l=180.00n m=1
T5 w=3.4u l=180.00n m=1
T6 w=1.7u l=180.00n m=1
T13 w=9.4u l=180.00n m=1
T15 w=5.0u l=180.00n m=1
T7 w=5.0u l=180.00n m=1
T8 w=3.4u l=180.00n m=1
T12 w=2.16u l=0.18n m=1
T16 w=9.4u l=180.00n m=1
T10 w=2.16u l=0.18n m=1
T4 w=2.16u l=0.18n m=1
T1 w=3.6u l=0.18n m=1
T9 w=2.16 l=0.18n m=1
T3 w=2.16u l=0.18n m=1
T0 w=3.6u l=0.18n m=1
T2 w=3.6u l=0.18n m=1
T11 w=2.16u l=0.18n m=1
DATAN
DATA
CLK

20ET20 ES096660

FIG. 9

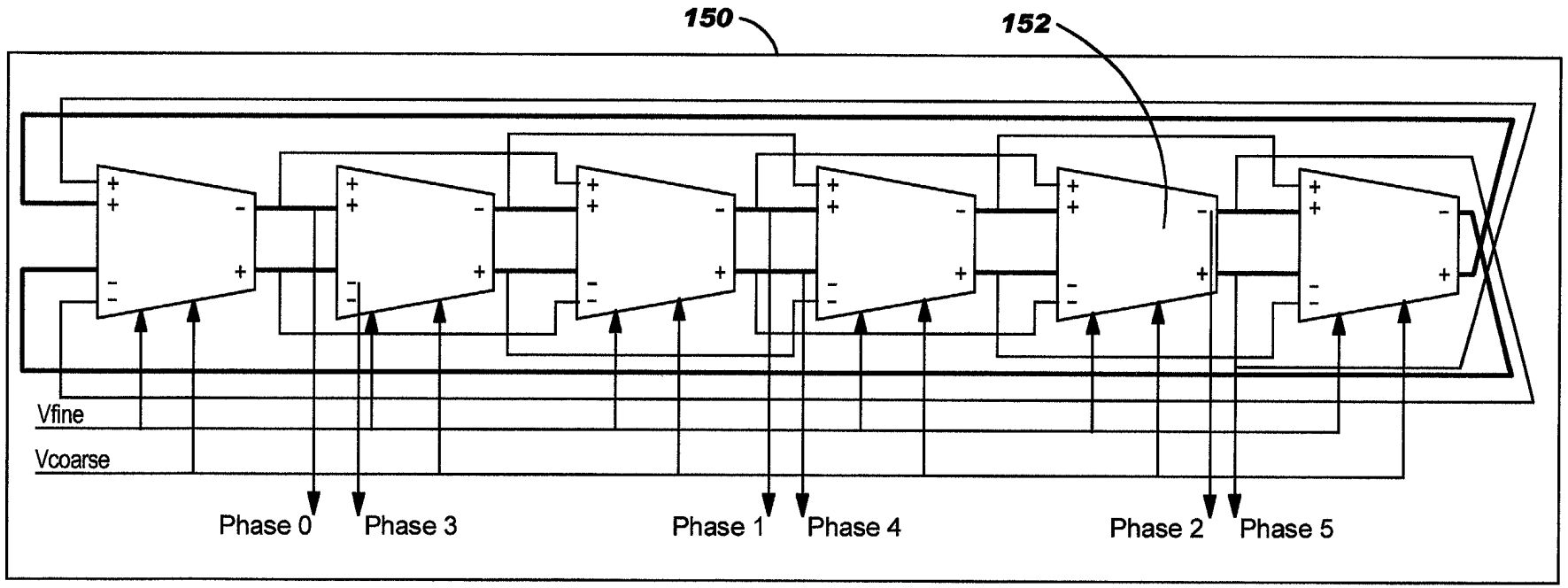
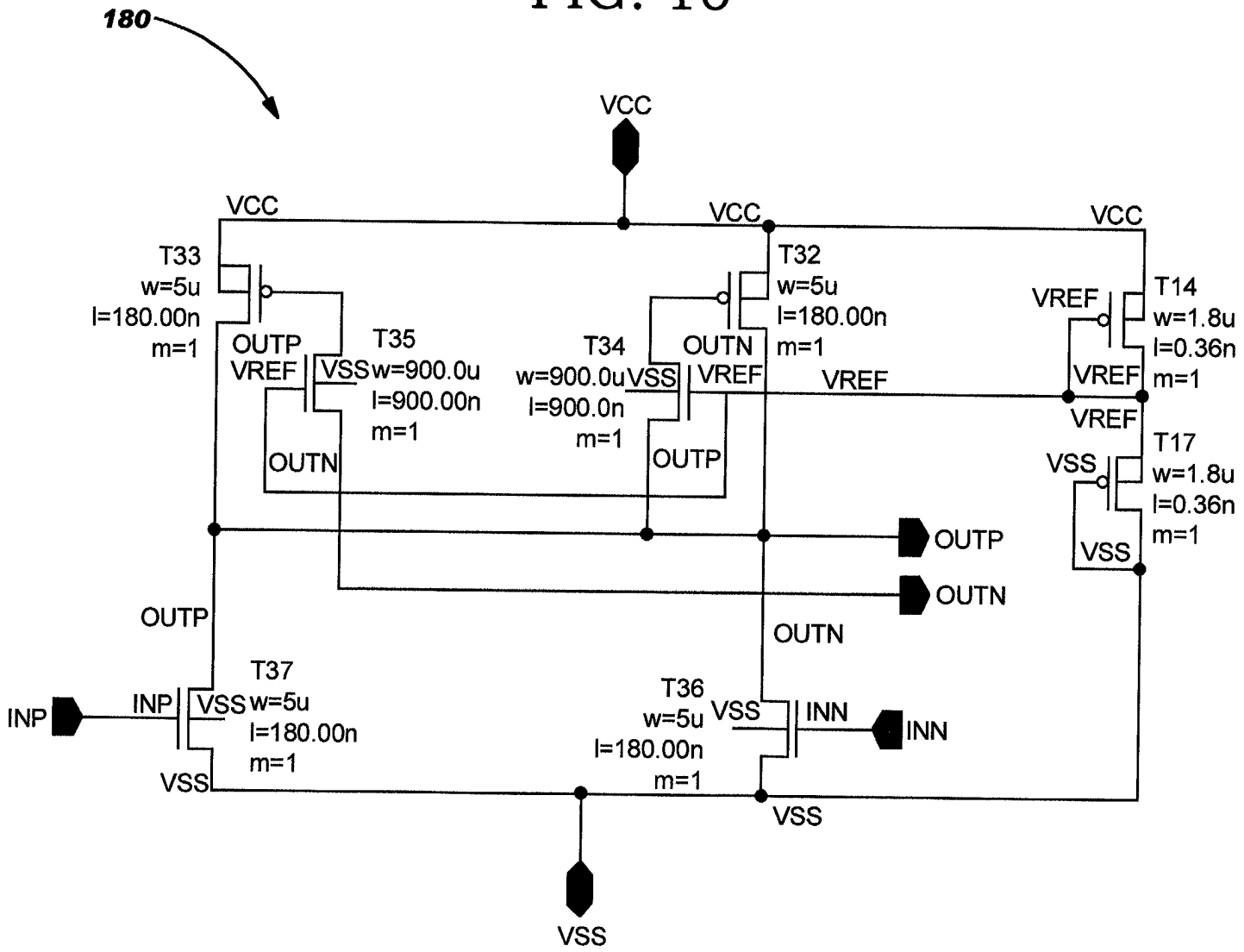


FIG. 10



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FIG. 11

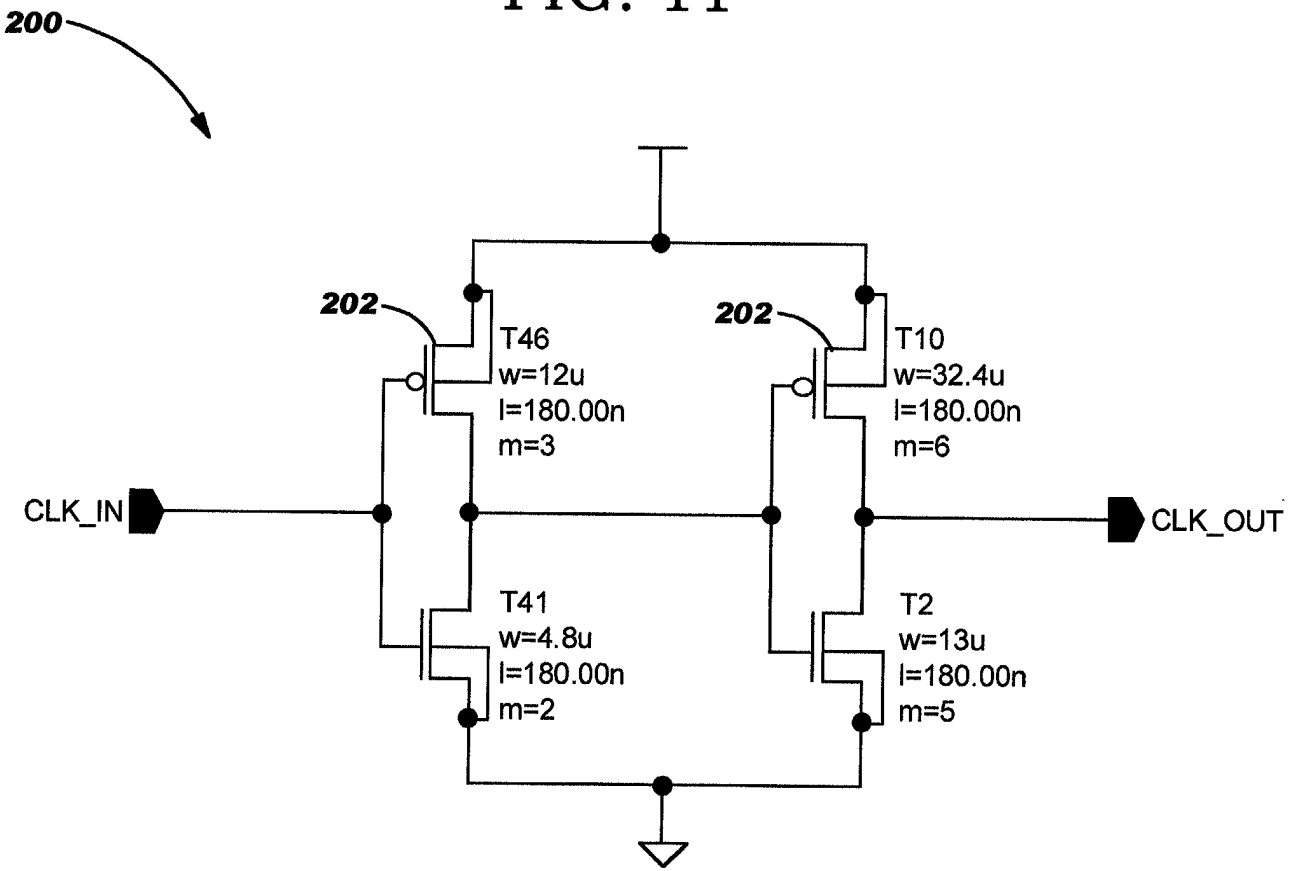

200
202
T46
w=12u
l=180.00n
m=3
202
T10
w=32.4u
l=180.00n
m=6
CLK_IN
CLK_OUT
T41
w=4.8u
l=180.00n
m=2
T2
w=13u
l=180.00n
m=5

FIG. 12

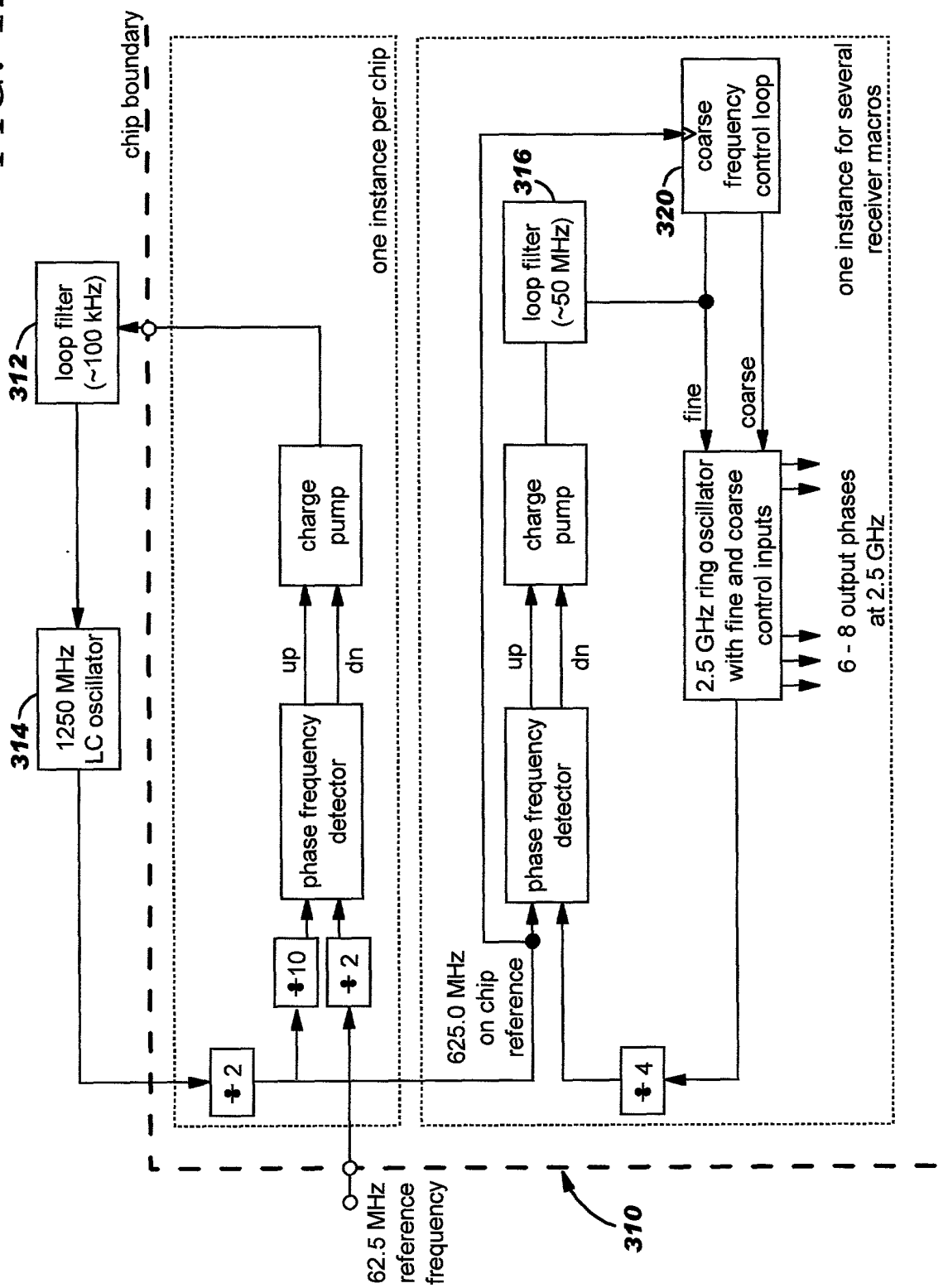
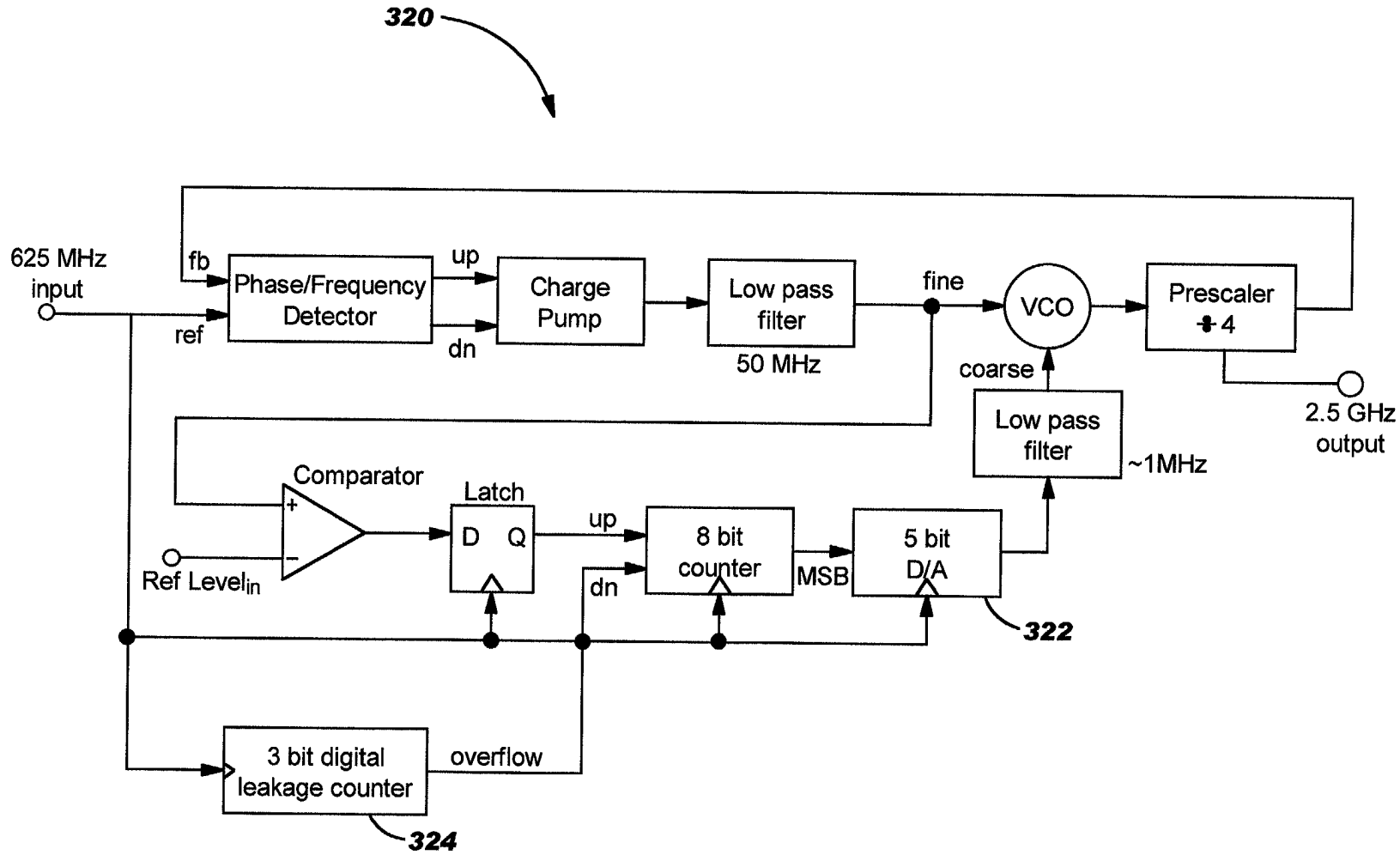

chip boundary
one instance per chip
one instance for several receiver macros
312
loop filter (~100 kHz)
314
1250 MHz LC oscillator
÷ 2
÷10
÷ 2
phase frequency detector
charge pump
up
dn
62.5 MHz reference frequency
310
625.0 MHz on chip reference
316
loop filter (~50 MHz)
320
coarse frequency control loop
fine
coarse
2.5 GHz ring oscillator with fine and coarse control inputs
÷ 4
6 - 8 output phases at 2.5 GHz

FIG. 13



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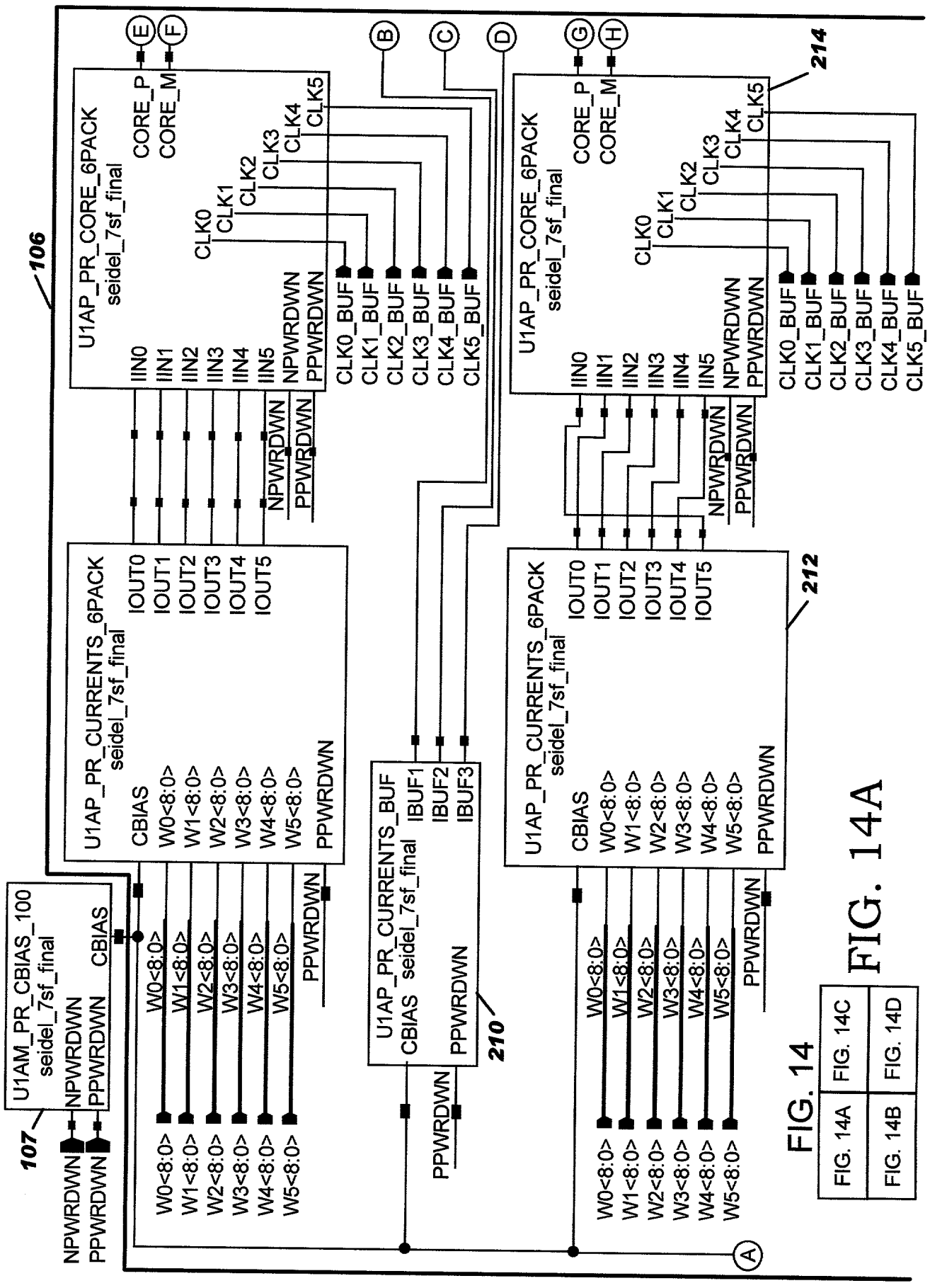


FIG. 14

FIG. 14A	FIG. 14C
FIG. 14B	FIG. 14D

FIG. 14A

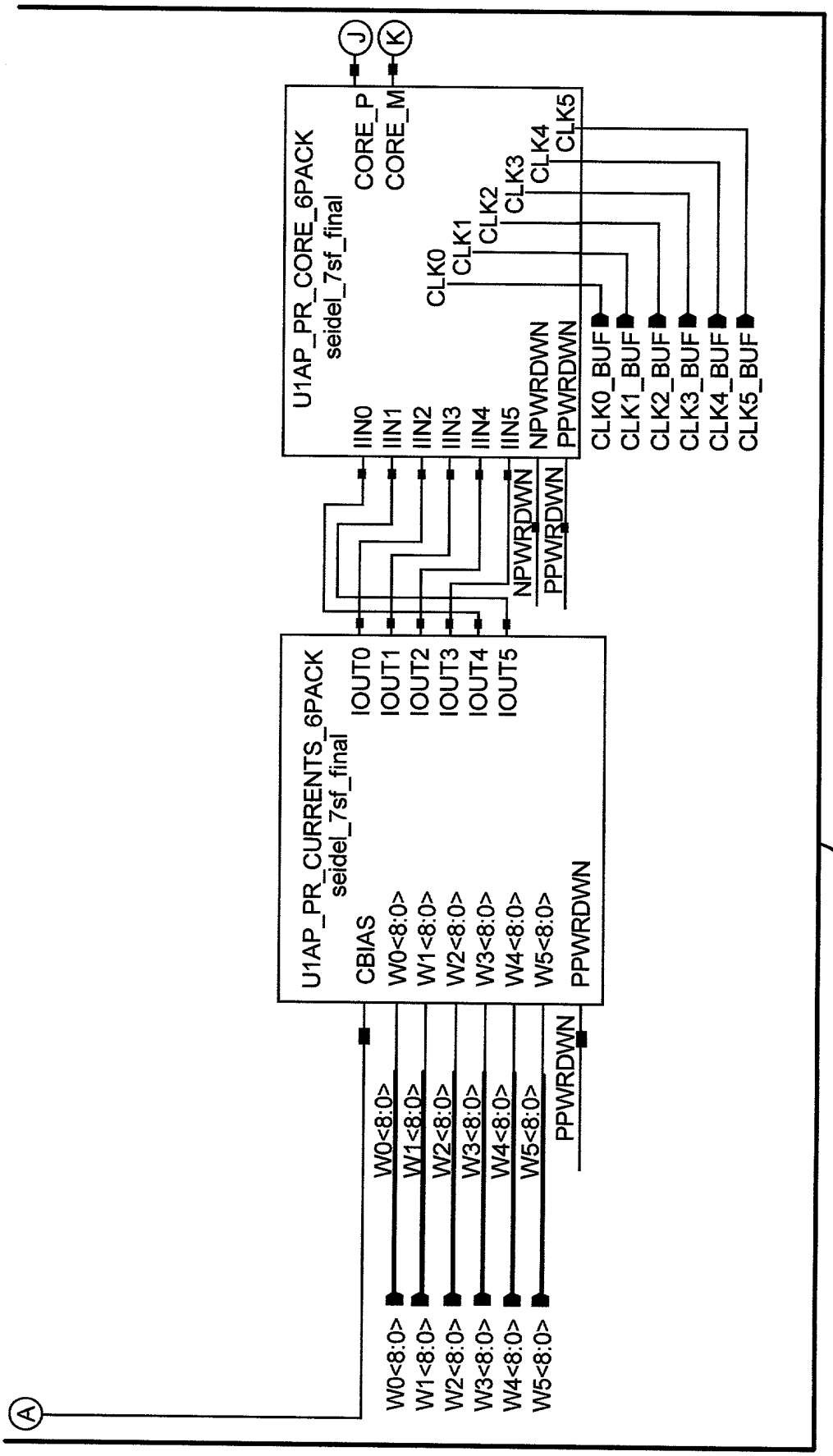
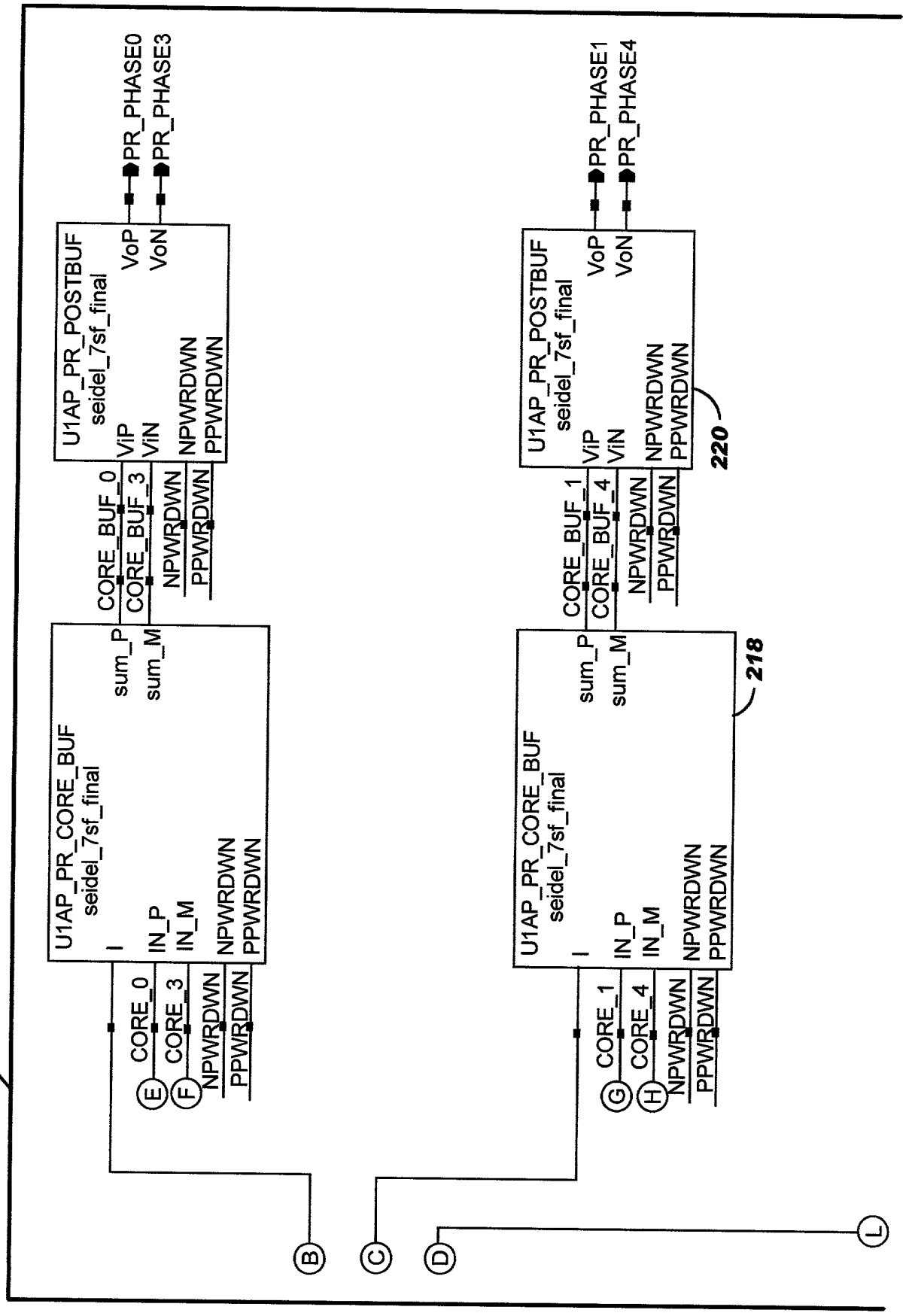

A
J
K
U1AP_PR_CORE_6PACK
seidel_7sf_final
CORE_P
CORE_M
IIN0
IIN1
IIN2
IIN3
IIN4
IIN5
NPWRDWN
PPWRDWN
CLK0
CLK1
CLK2
CLK3
CLK4
CLK5
CLK0_BUF
CLK1_BUF
CLK2_BUF
CLK3_BUF
CLK4_BUF
CLK5_BUF
U1AP_PR_CURRENTS_6PACK
seidel_7sf_final
CBIAS
IOUT0
IOUT1
IOUT2
IOUT3
IOUT4
IOUT5
W0<8:0>
W1<8:0>
W2<8:0>
W3<8:0>
W4<8:0>
W5<8:0>
PPWRDWN
106

FIG. 14B

FIG. 14C


108
U1AP_PR_CORE_BUF
seidel_7sf_final
I
IN_P
IN_M
NPWRDWN
PPWRDWN
sum_P
sum_M
CORE_0
CORE_3
CORE_1
CORE_4
U1AP_PR_POSTBUF
seidel_7sf_final
ViP
ViN
VoP
VoN
CORE_BUF_0
CORE_BUF_3
CORE_BUF_1
CORE_BUF_4
PR_PHASE0
PR_PHASE3
PR_PHASE1
PR_PHASE4
218
220
B
C
D
E
F
G
H
L

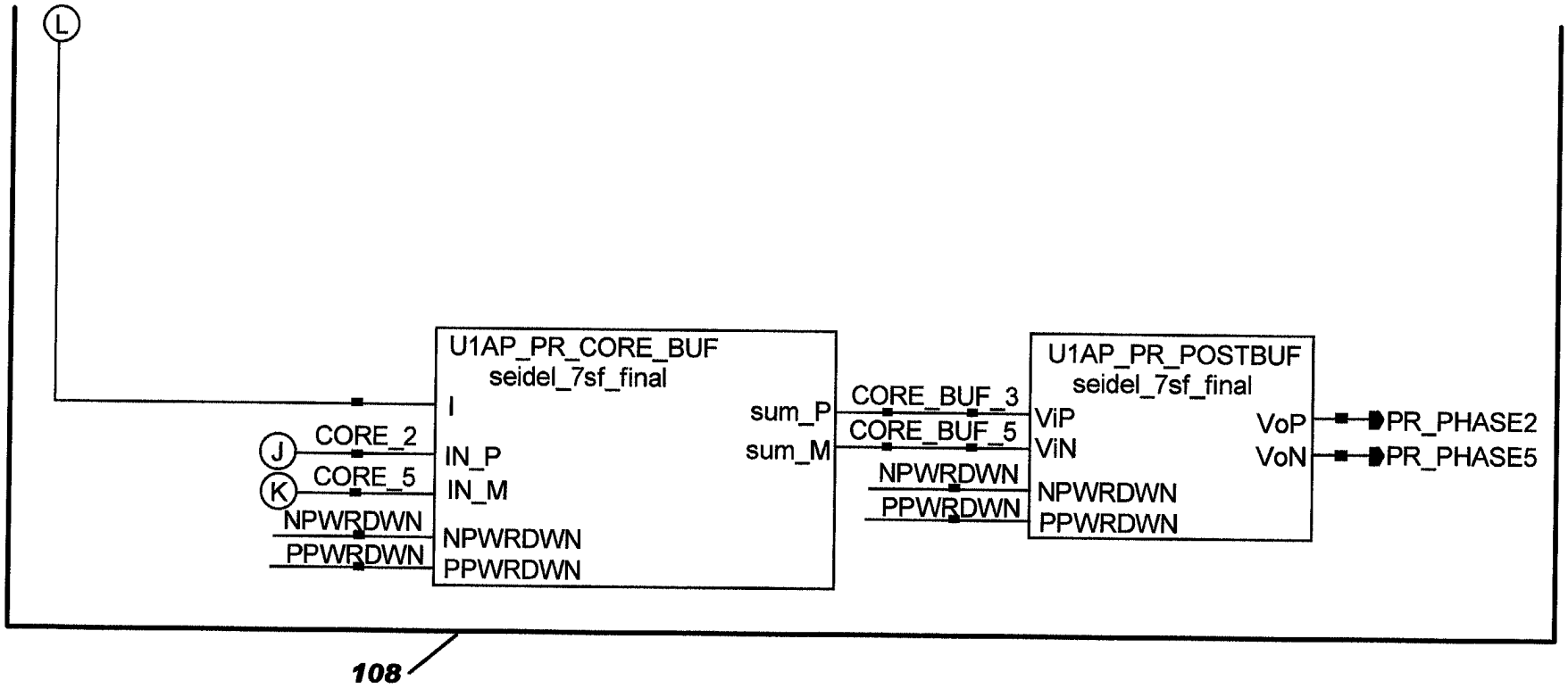

L
U1AP_PR_CORE_BUF
seidel_7sf_final
I
sum_P
sum_M
J
CORE_2
IN_P
K
CORE_5
IN_M
NPWRDWN
NPWRDWN
PPWRDWN
PPWRDWN
CORE_BUF_3
CORE_BUF_5
NPWRDWN
PPWRDWN
U1AP_PR_POSTBUF
seidel_7sf_final
ViP
ViN
NPWRDWN
PPWRDWN
VoP
VoN
PR_PHASE2
PR_PHASE5
108

FIG. 14D

FIG. 15

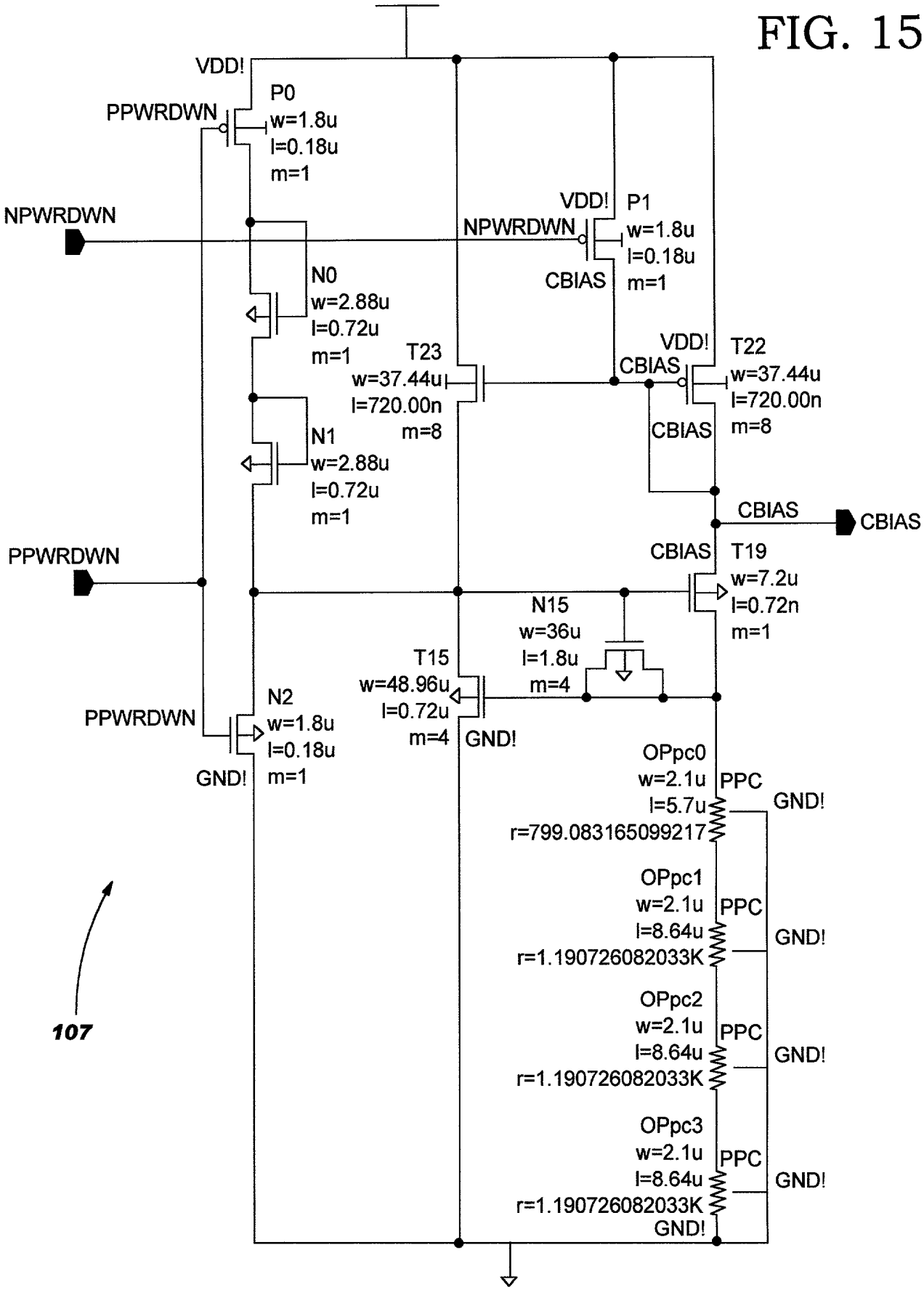
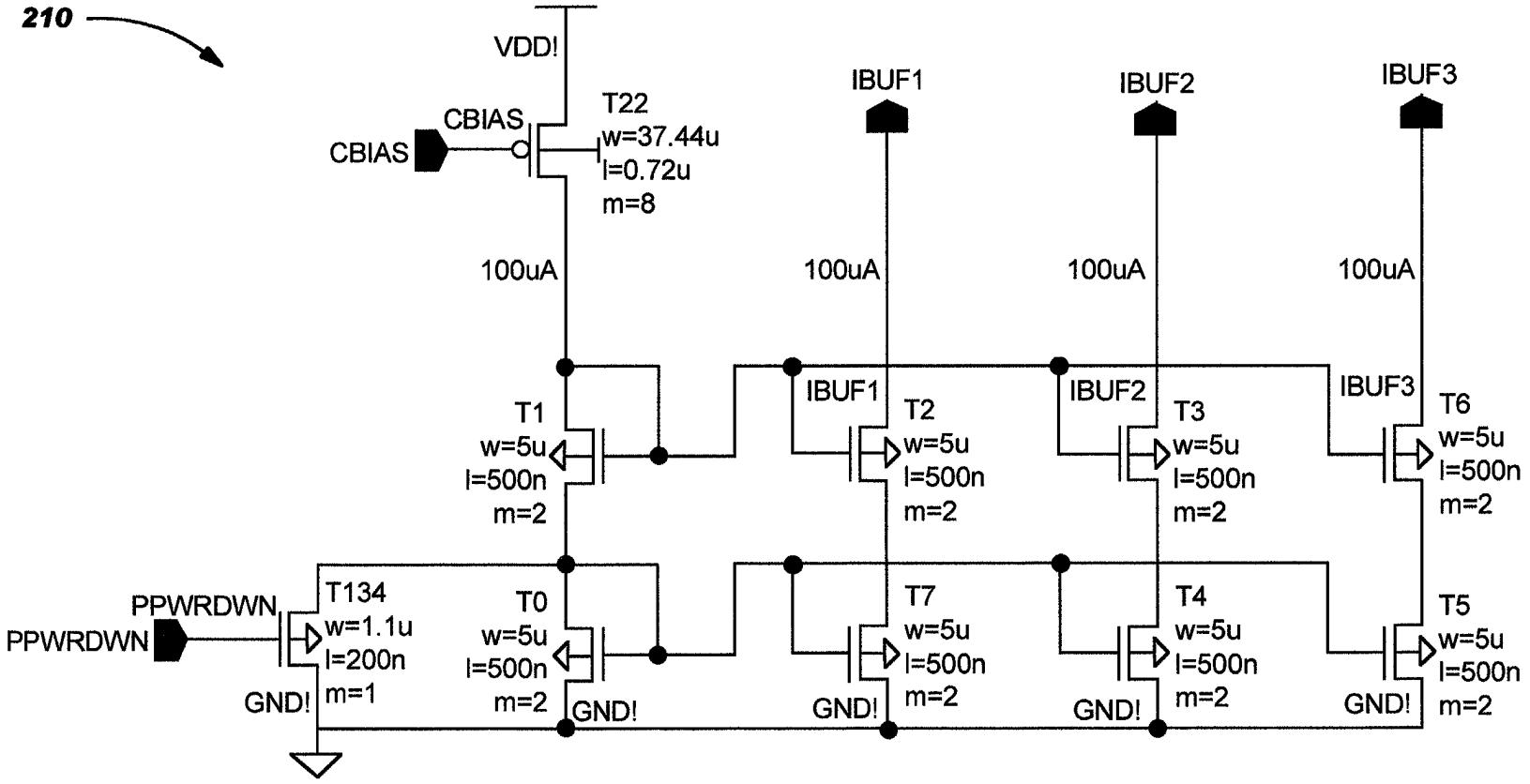

VDD!
P0
PPWRDWN
w=1.8u
l=0.18u
m=1
NPWRDWN
VDD!
P1
NPWRDWN
w=1.8u
l=0.18u
CBIAS
m=1
N0
w=2.88u
l=0.72u
m=1
T23
w=37.44u
l=720.00n
m=8
VDD!
T22
CBIAS
w=37.44u
l=720.00n
m=8
CBIAS
N1
w=2.88u
l=0.72u
m=1
CBIAS
CBIAS
PPWRDWN
CBIAS
T19
w=7.2u
l=0.72n
m=1
N15
w=36u
l=1.8u
m=4
T15
w=48.96u
l=0.72u
m=4
GND!
N2
PPWRDWN
w=1.8u
l=0.18u
GND!
m=1
OPpc0
w=2.1u
l=5.7u
r=799.083165099217
PPC
GND!
OPpc1
w=2.1u
l=8.64u
r=1.190726082033K
PPC
GND!
OPpc2
w=2.1u
l=8.64u
r=1.190726082033K
PPC
GND!
OPpc3
w=2.1u
l=8.64u
r=1.190726082033K
PPC
GND!
GND!
107

FIG. 16



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FIG. 17

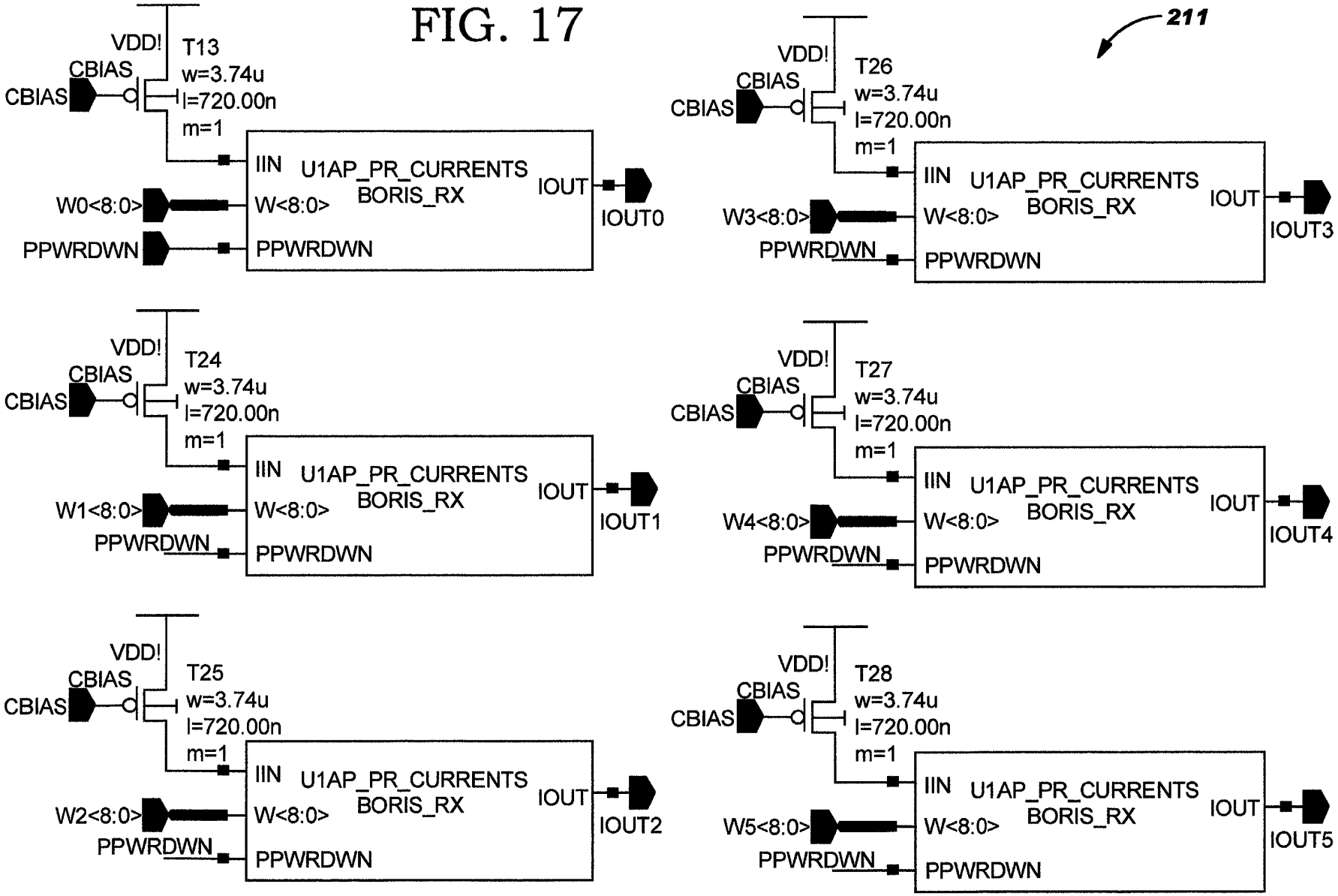
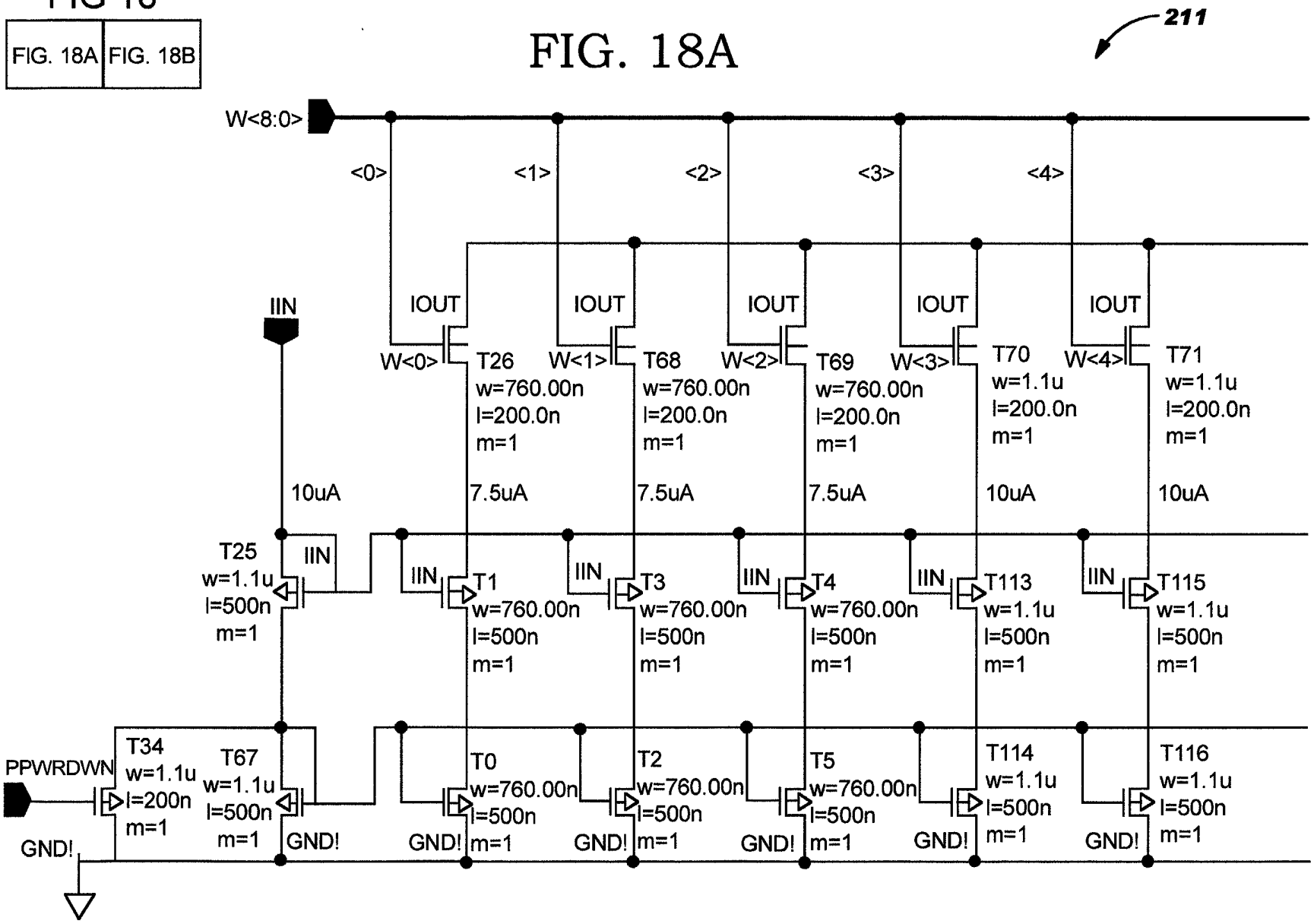

211
VDD!
CBIAS
T13
w=3.74u
l=720.00n
m=1
IIN
U1AP_PR_CURRENTS
BORIS_RX
IOUT
IOUT0
W0<8:0>
W<8:0>
PPWRDWN
PPWRDWN
T26
IOUT3
W3<8:0>
T24
IOUT1
W1<8:0>
T27
IOUT4
W4<8:0>
T25
IOUT2
W2<8:0>
T28
IOUT5
W5<8:0>

FIG 18

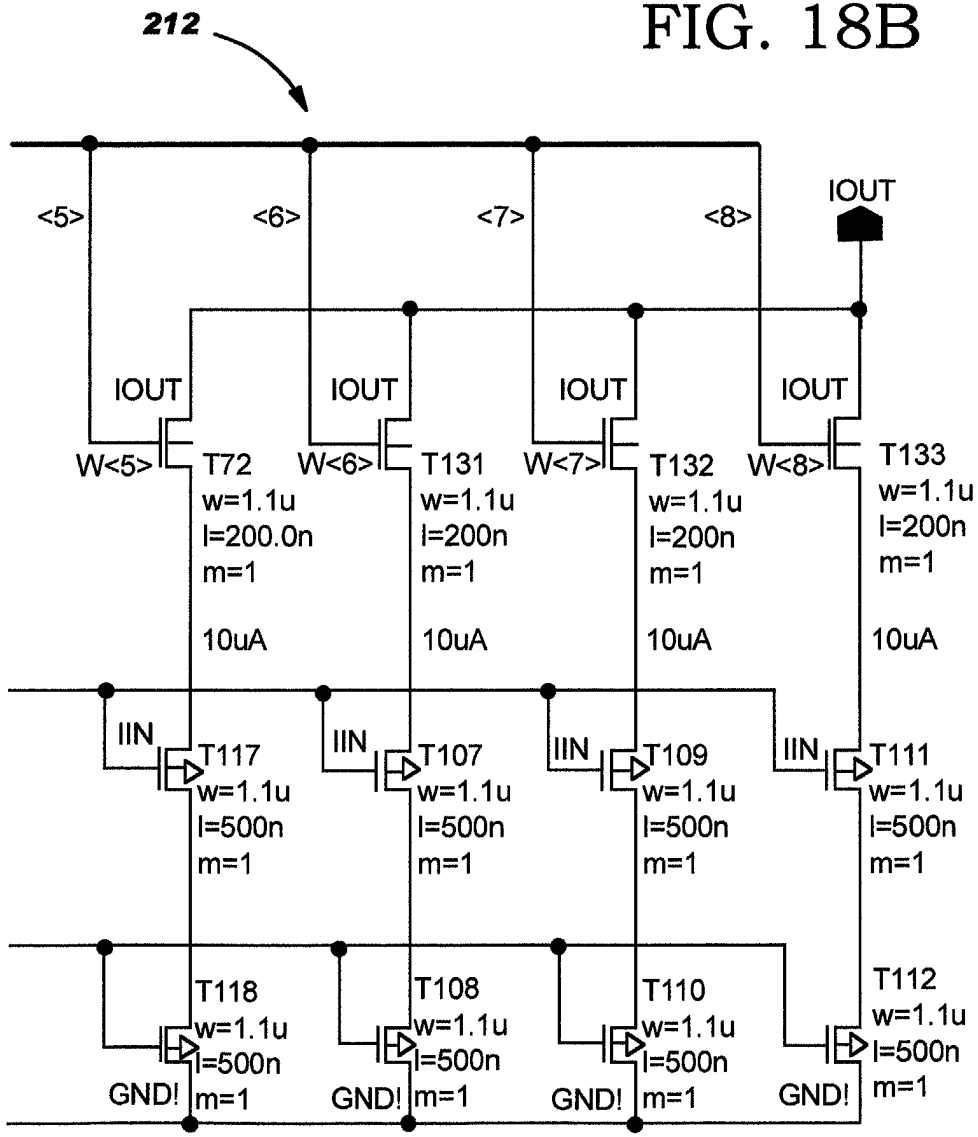
FIG. 18A	FIG. 18B

FIG. 18A



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FIG. 18B



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FIG. 19

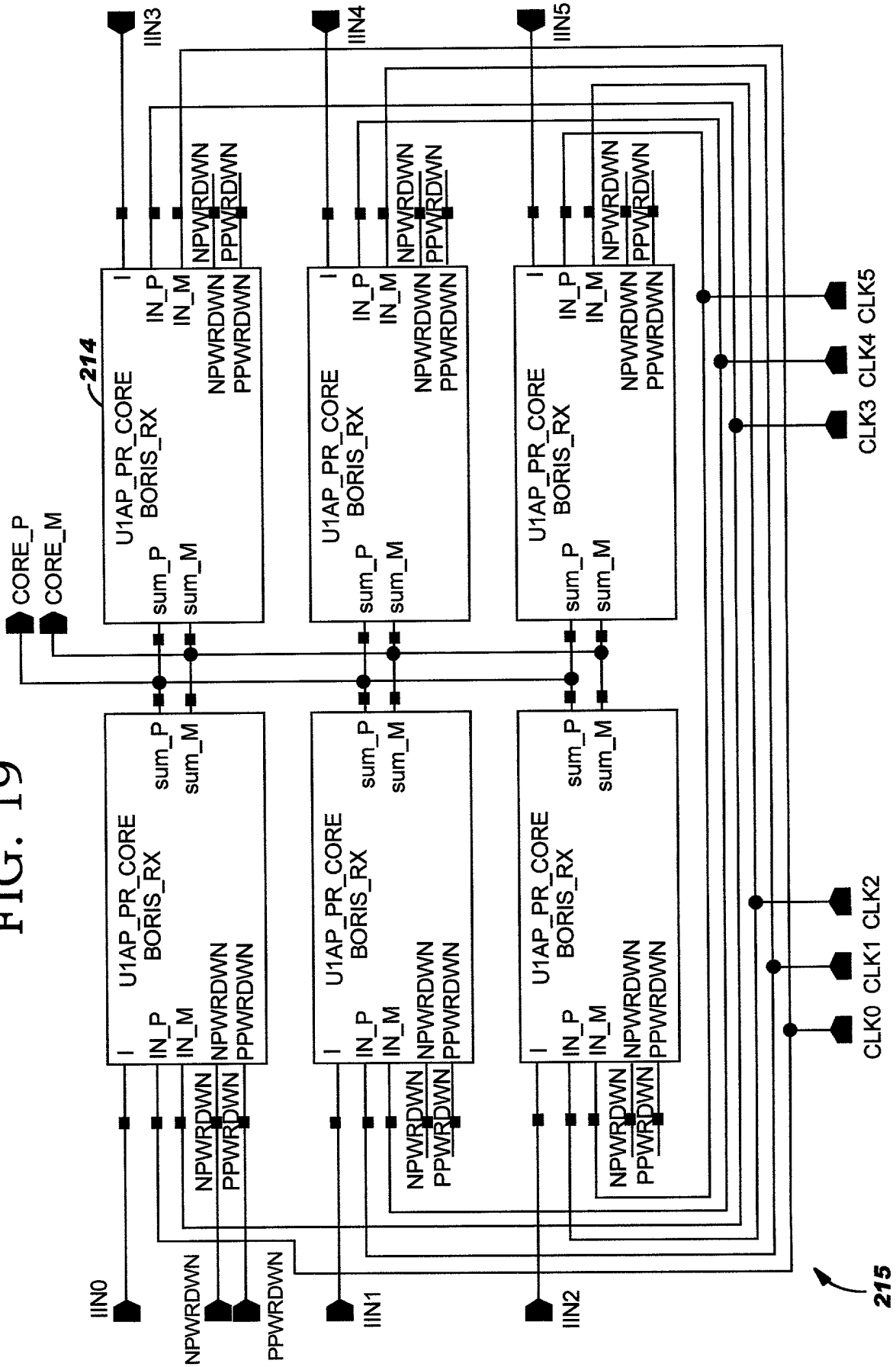

IIN0
IIN1
IIN2
IIN3
IIN4
IIN5
NPWRDWN
PPWRDWN
CORE_P
CORE_M
CLK0 CLK1 CLK2
CLK3 CLK4 CLK5
214
215
U1AP_PR_CORE
BORIS_RX
I
IN_P
IN_M
sum_P
sum_M

FIG. 20

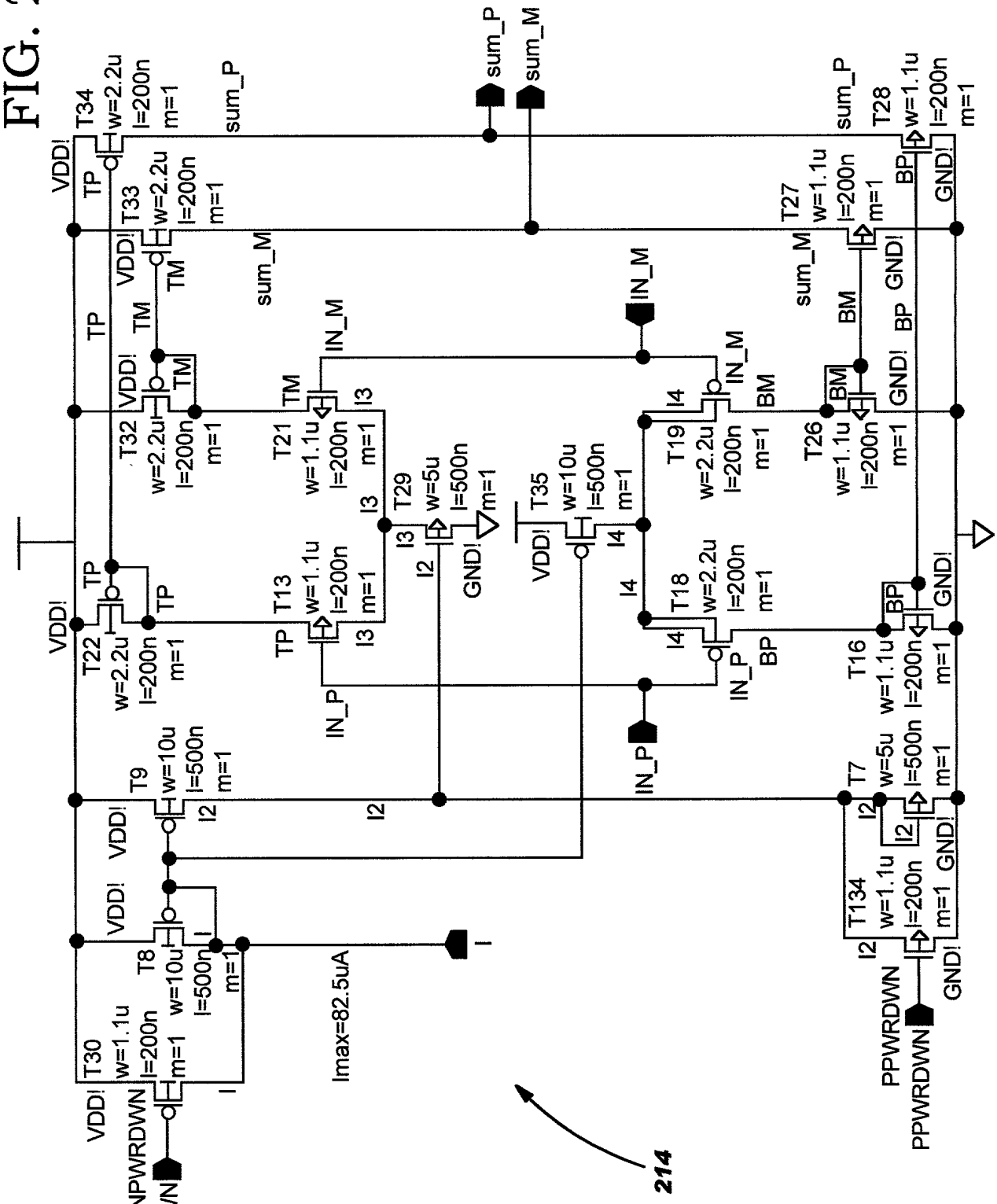

VDD!
GND!
sum_P
sum_M
IN_M
IN_P
NPWRDWN
PPWRDWN
Imax=82.5uA
214
T7
T8
T9
T13
T16
T18
T19
T21
T22
T26
T27
T28
T29
T30
T32
T33
T34
T35
T134
w=1.1u
w=2.2u
w=5u
w=10u
l=200n
l=500n
m=1

FIG. 21

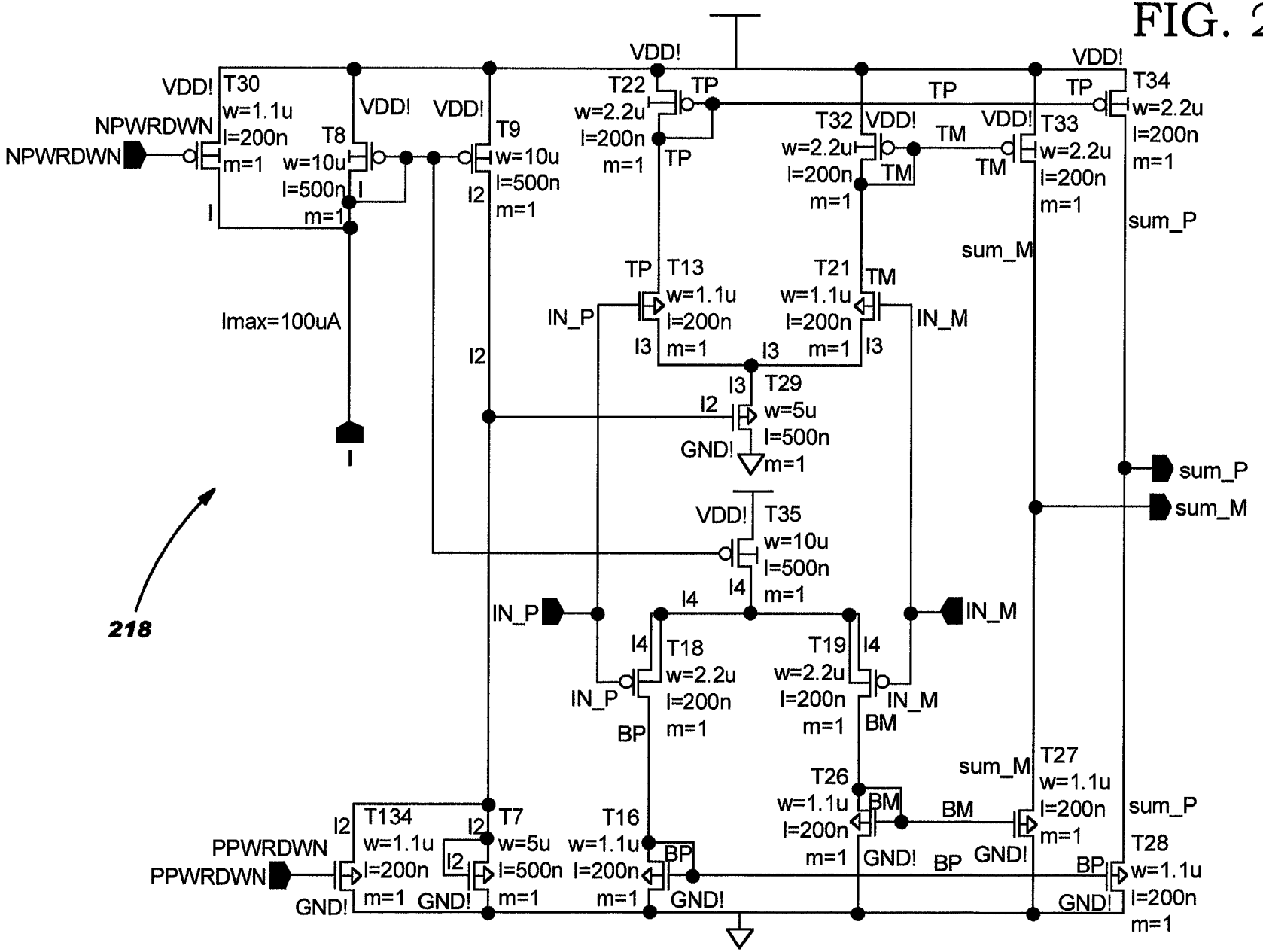

VDD!
T30
w=1.1u
l=200n
m=1
NPWRDWN
T8
w=10u
l=500n
m=1
T9
w=10u
l=500n
m=1
T22
w=2.2u
l=200n
m=1
TP
T32
w=2.2u
l=200n
m=1
TM
T33
w=2.2u
l=200n
m=1
T34
w=2.2u
l=200n
m=1
sum_P
sum_M
Imax=100uA
T13
w=1.1u
l=200n
m=1
T21
w=1.1u
l=200n
m=1
IN_P
IN_M
I2
I3
T29
w=5u
l=500n
m=1
GND!
T35
w=10u
l=500n
m=1
I4
T18
w=2.2u
l=200n
m=1
T19
w=2.2u
l=200n
m=1
BP
BM
T26
w=1.1u
l=200n
m=1
T27
w=1.1u
l=200n
m=1
T28
w=1.1u
l=200n
m=1
T134
w=1.1u
l=200n
m=1
T7
w=5u
l=500n
m=1
T16
w=1.1u
l=200n
m=1
PPWRDWN
218

FIG. 22

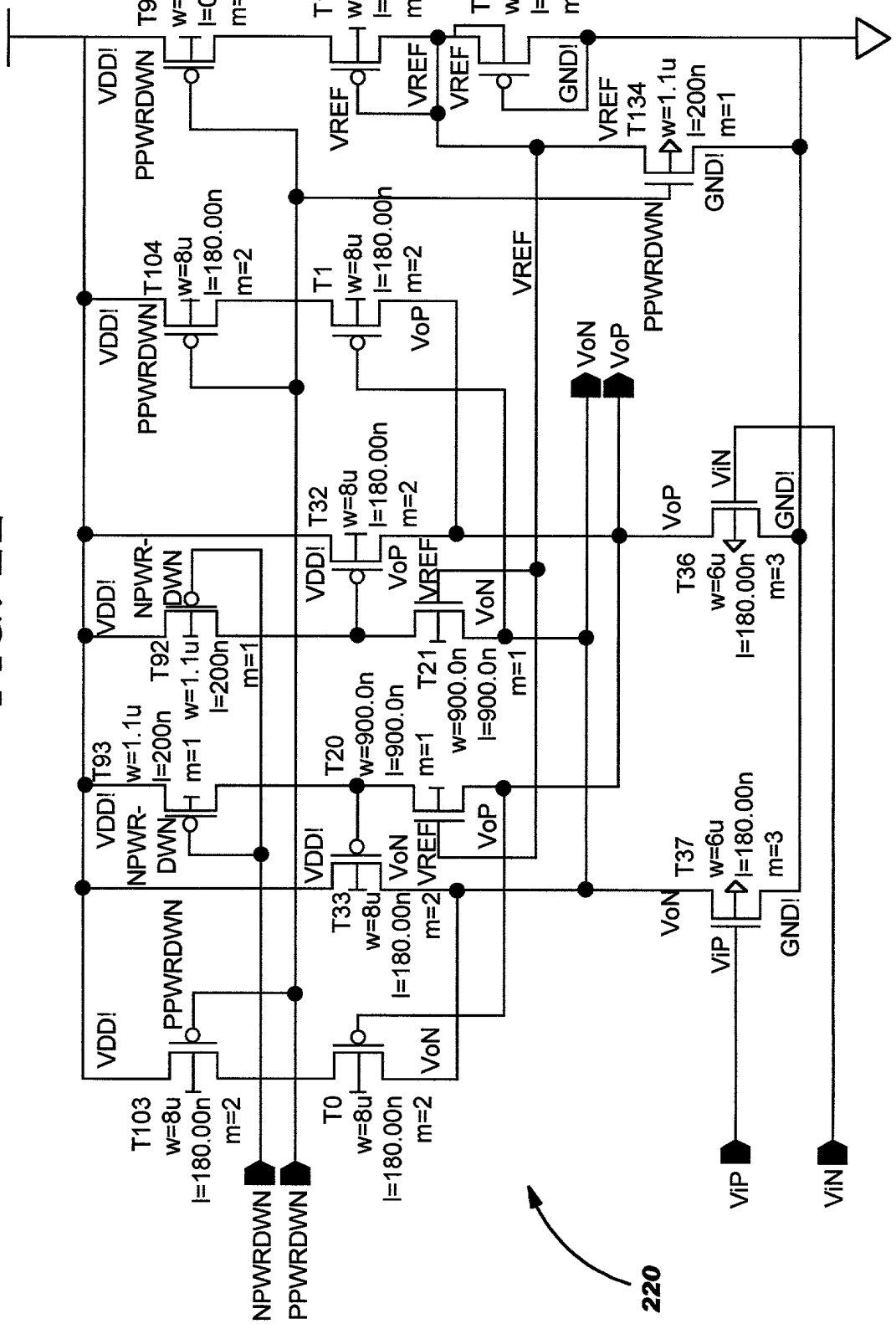
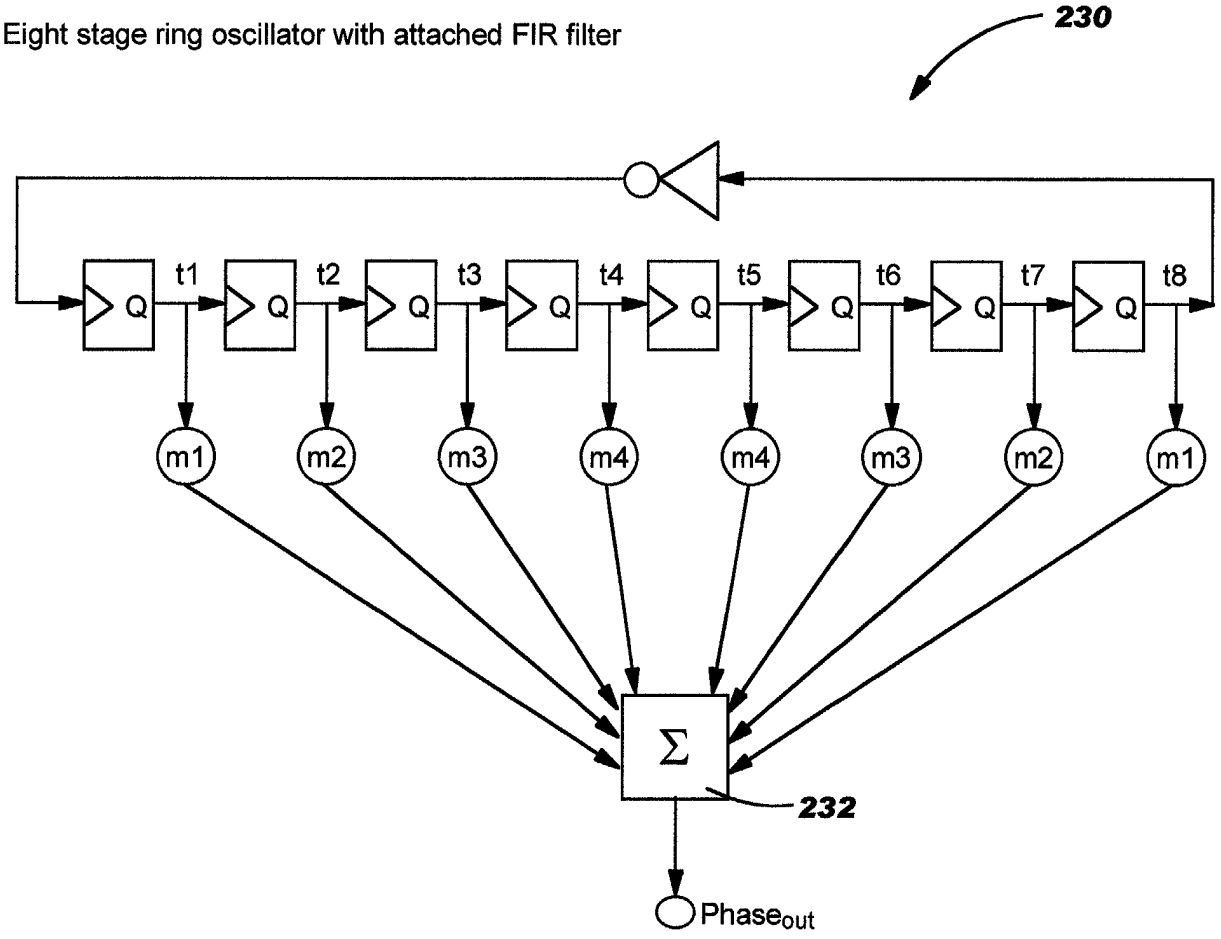

T95 w=1.8u l=0.36u m=1
T14 w=1.8u l=0.36n m=1
T89 w=1.8u l=0.36n m=1
T134 w=1.1u l=200n m=1
T104 w=8u l=180.00n m=2
T1 w=8u l=180.00n m=2
T32 w=8u l=180.00n m=2
T92 w=1.1u l=200n m=1
T93 w=1.1u l=200n m=1
T20 w=900.0n l=900.0n m=1
T21 w=900.0n l=900.0n m=1
T36 w=6u l=180.00n m=3
T37 w=6u l=180.00n m=3
T33 w=8u l=180.00n m=2
T103 w=8u l=180.00n m=2
T0 w=8u l=180.00n m=2
VDD!
GND!
VREF
VoP
VoN
ViP
ViN
PPWRDWN
NPWR-DWN
NPWRDWN
220

FIG. 23

Eight stage ring oscillator with attached FIR filter



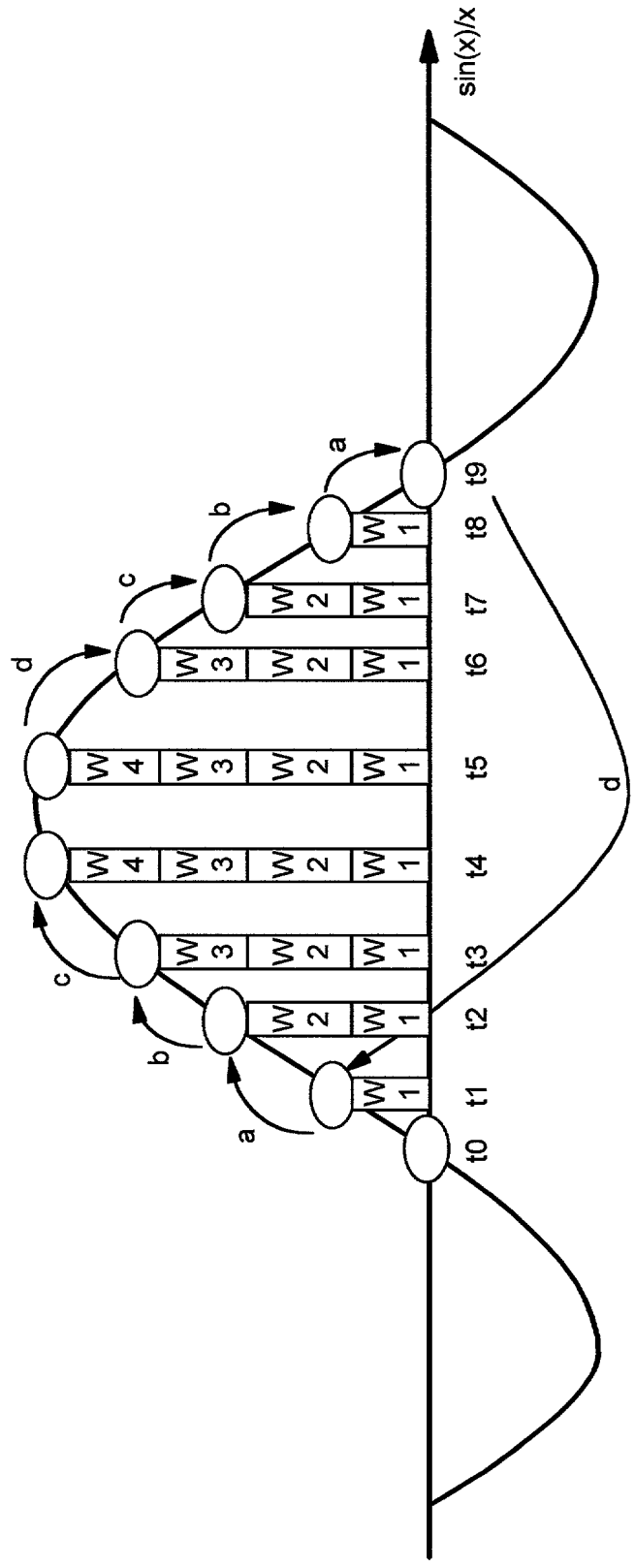


FIG. 24

Rotation by one phase slice in four steps (a) to (d)

FIG. 25

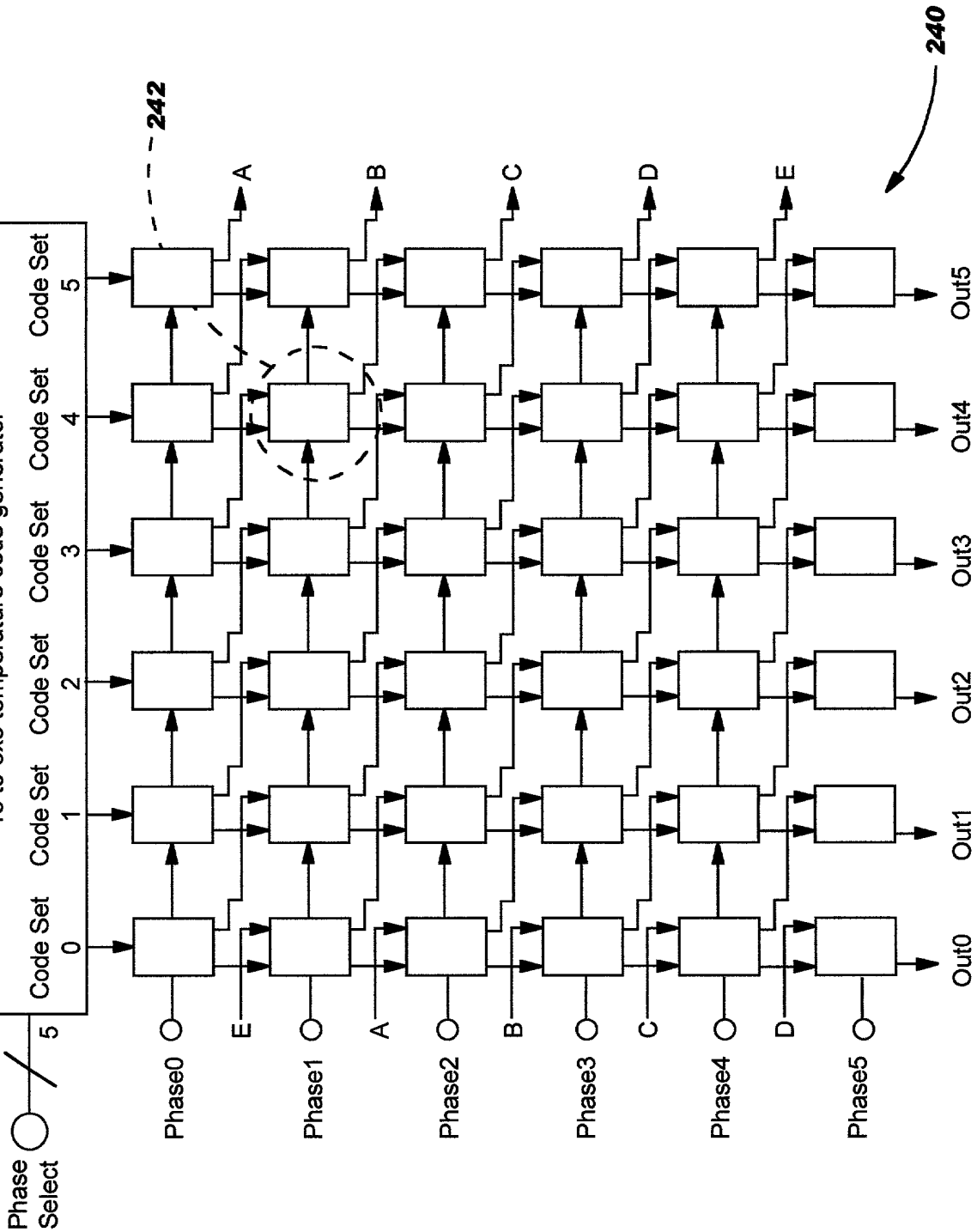
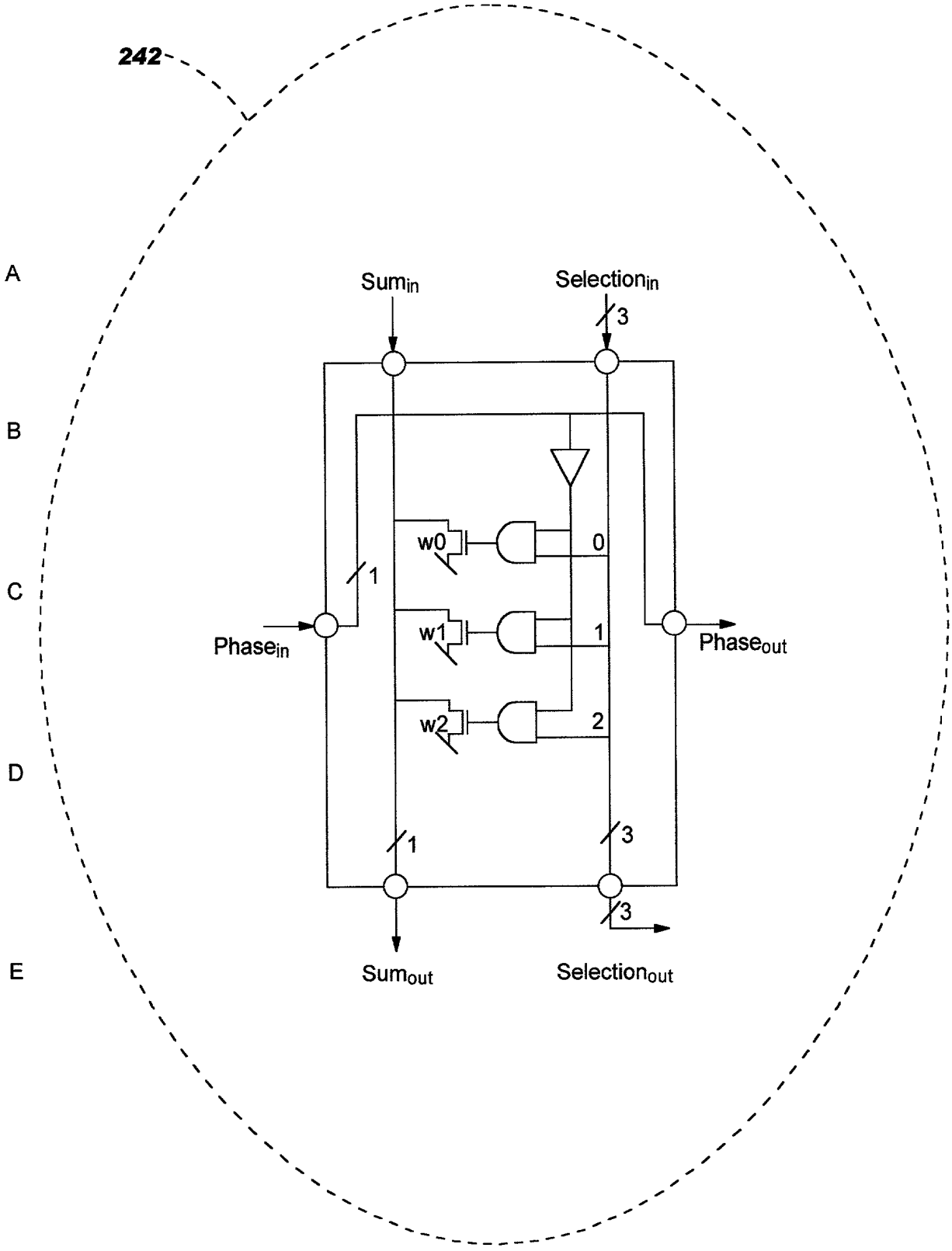

240
242
18 to 6x3 temperature code generator
Code Set 0
Code Set 1
Code Set 2
Code Set 3
Code Set 4
Code Set 5
Phase Select
5
Phase0
Phase1
Phase2
Phase3
Phase4
Phase5
A
B
C
D
E
Out0
Out1
Out2
Out3
Out4
Out5

FIG. 26


242
A
B
C
D
E
Sum_in
Selection_in
3
w0
0
1
w1
1
Phase_in
Phase_out
w2
2
1
3
3
Sum_out
Selection_out